เป็นหนังสือภาษาอังกฤษ

รายงานวิจัยฉบับสมบูรณ์

โครงการ

วงจรกรองแบบเวลาต่อเนื่องสำหรับระบบสื่อสารแบบไร้สายโดยใช้รูปแบบของทรานคอนดัคเตอร์ (แบบป้อนกลับกระแส) -ตัวเก็บประจุ

High-Order Continuous-Time Filters employing Current-Feedback Transconductor-Capacitor Structure in CMOS Technology for Wireless Communications

โดย

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ธันวาคม 2550

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ABSTRACT

Investigation on various aspects of integrated filter design in CMOS technology under low supply voltage is presented.

A resistive source-degeneration CMOS transconductor with excellent linearity utilizing current-feedback has been described. The technique adds minimum complexity (just two or four additional transistors) to enhance linearity without extra current consumption, in other words high transconductance/current efficiency of an ordinary source degeneration transconductor is preserved but with superior linearity performance. The transconductance's polarity inversion of Caprio's quad has also been solved by adding another cross-coupling transistor pair.

A 1.8V CMOS dual-mode fifth-order polyphase GmC filter for Bluetooth/ZigBee transceiver has been designed. The complex bandpass filter is based on Gm-C filter structure with appropriate crossing transconductors to shift lowpass response to the required IF frequencies. It deploys a simple source degeneration transconductor integrated with a network, which could simultaneously provide common-mode stability and dc gain enhancement.

High-gain current amplifiers have been successfully employed as an alternative active building block to conventional operational amplifiers or operational transconductance amplifier in MOSFET-C and active-RC filters. The second-order filters employing the proposed current amplifiers render better linearity performance over the conventional folded-cascode OTA.

A compact OTA suitable for low voltage filter implementations has been developed. The circuit relies primarily on the feed-forward class AB output stage that features low supply operation and common-mode rejection at no cost to transconductance/bias-current efficiency. It is envisaged that the feed-forward output configuration could be applied to current-mode circuits in general or any other circuits with output current variables, such as transconductor (G_m), current conveyor etc. Verified through extensive simulation, it was demonstrated that a low supply voltage filter with a competitive FoM performance at small complexity is entirely viable with the use of the OTA structure.

Two different methods have been presented, basing on state-space and element substitution, to transform the real Gm-C filters with floating capacitors into the corresponding complex Gm-C filters. The resulting complex filter structure is suitable for fully-differential implementation using widely-used fully-differential transconductors. To demonstrate the proposed method, the fully-differential complex Gm-C filter was realized from the 3rd-order elliptic Gm-C filter. It was found that with the same frequency specifications, the elliptic complex filter derived from the proposed method outperforms the Butterworth and Chebyshev complex filters in terms of noise, linearity, area, and power consumption.

บทคัดย่อ

โครงการวิจัยนี้ได้ทำงานศึกษาเทคนิคต่างๆที่เป็นประโยชน์ในการออกแบบวงจรกรองความถี่ในเทคโนโลยีซีมอสสำหรับใช้งานภายใต้ไฟเลี้ยงต่ำ

วงจรทรานส์คอนดัคเตอร์แบบซอสดีเจนเนอเรชั่นที่ใช้ตัวต้านทานและมีความเป็นเชิงเส้นสูงโดยอาศัยหลักการป้อนกลับซึ่งส่งผลในการกำจัดความไม่เป็นเชิงเส้นของทรานซิสเตอร์และไม่มีการใช้กำลังงานเพิ่มเมื่อเทียบกับเทคนิคเดิม นอกจากนี้ได้มีการเสริมวงจรเพิ่มเพื่อทำให้ขั้วของวงจรเป็นบวกเสมอเพื่อป้องกันปัญหาเสถียรภาพของวงจรเมื่อนำไปใช้ในวงจรกรอง

ได้ทำการออกแบบวงจรกรองเชิงซ้อนโดยใช้เทคนิคทรานส์คอนดัคเตอร์-ตัวเก็บประจุสำหรับภาครับของระบบบลูทูธและซิกบี วงจรกรองดังกล่าวเป็นแบบเซพบีเซพลำดับห้าและทำงานภายใต้ไฟเลี้ยง 1.8 โวลต์ ได้มีการใช้เทคนิคเพื่อรับรองเสถียรภาพสำหรับโหมดร่วมของวงจรพร้อมกับการเพิ่มอัตราขยาย

ได้ทำการออกแบบวงจรขยายกระแสที่มีอัตราขยายสูงสำหรับการออกแบบวงจรกรองแบบมอสเฟต-ซีหรือแบบแอคทีฟ-ตัวต้านทาน/ตัวเก็บประจุ ซึ่งวงจรดังกล่าวทำหน้าที่แทนออปแอมป์หรือวงจรขยายทรานส์คอนดัคแตนซ์ (โอทีเอ) ได้มีการเปรียบเทียบประสิทธิภาพการทำงานกับวงจรโอทีเอแบบพับดั้งเดิมและพบว่าวงจรที่นำเสนอให้วงจรกรองที่มีความเป็นเชิงเส้นสูงกว่า

มีการออกแบบโอทีเอขนาดเล็กซึ่งเหมาะสำหรับวงจรกรองที่ใช้ไฟเลี้ยงต่ำ วงจรดังกล่าวอาศัยหลักการป้อนไปด้านหน้าซึ่งทำงานในแบบคลาสเอบี โครงสร้างดังกล่าวสามารถขจัดสัญญาณโหมดร่วมได้โดยไม่สูญเสียอัตราขยายและไม่มีความจำเป็นต้องสูญเสียกำลังงานเพิ่ม ซึ่งเทคนิคดังกล่าวสามารถนำไปประยุกต์ใช้กับวงจรที่มีกระแสเป็นตัวแปรด้านออกเช่น ทรานส์คอนดัคเตอร์ วงจรสายพานกระแส

นำเสนอสองวิธีการสำหรับการออกแบบวงจรกรองเชิงซ้อนที่แปลงมาจากต้นแบบวงจรกรองผ่านความถี่ต่ำแบบทรานส์คอนดัคเตอร์-ตัวเก็บประจุที่มีตัวเก็บประจุลอยเช่นแบบอีลิปติกคือวิธีเสตท-เสปซและวิธีแทนตัวอุปกรณ์ เทคนิคที่นำเสนอเหมาะสำหรับวงจรผลต่างแบบสมดุลซึ่งสามารถนำทรานส์คอนดัคเตอร์ทั่วๆไปมาใช้ได้ ตัวอย่างการออกแบบได้นำเสนอผ่านวงจรอีลิปติกอันดับสามซึ่งก็ได้แสดงให้เห็นว่าด้วยประสิทธิภาพการกรองที่เท่าเทียมกันวงจรที่นำเสนอสามารถประหยัดกำลังงาน พื้นที่ซิลิกอนได้ดีกว่า มีสัญญาณรบกวนต่ำกว่า มีความเป็นเชิงเส้นสูงกว่า เมื่อเทียบกับวงจรที่สร้างมาจากต้นแบบเซฟบีเซฟอันดับห้าและวงจรบัตเตอร์เวิร์ธอันดับเก้า

บทสรุปสำหรับผู้บริหาร

โครงการวิจัยนี้นำเสนอเทคนิคการออกแบบวงจรสำหรับวงจรกรองความถี่ในเทคโนโลยีซีมอสสำหรับระบบสื่อสารไร้สายที่ใช้ไฟเลี้ยงต่ำ เทคโนโลยีที่ใช้มีขนาด 0.18 ไมครอนและมอสทราสซิสเตอร์มีแรงดันขีดเริ่มประมาณ 0.45โวลต์ เทคนิคที่คิดค้นนี้ได้ศึกษาสำหรับการประยุกต์ใช้กับวงจรกรองแบบทรานส์คอนดัคเตอร์-ตัวเก็บประจุและแบบแอคทีฟ-ตัวต้านทาน/ตัวเก็บประจุ สิ่งที่ได้นำเสนอนั้นคือ วงจรทรานส์คอนดัคเตอร์วงจรขยายทรานส์คอนดัคแตนซ์ปฏิบัติการ (โอทีเอ) วงจรขยายกระแสปฏิบัติการ การออกแบบวงจรกรองเชิงซ้อน การนำเสนอเทคนิคการป้อนไปด้านหน้าแบบโหมดผลต่างและโหมดร่วมซึ่งทำงานในคลาสเอบี

Executive Summary

This research presents various design techniques for integrated filters targeted for modern wireless communication chip operating under a low-voltage supply. The proposed techniques have been studied for Gm-C and active-RC filtering structures. And this renders useful circuit techniques for transconductors, operational transconductance amplifier (OTA), operational current amplifier, complex filters, and dual-mode (differential-mode and common-mode) feedforward techique working in class-AB.

Chapter 1

HIGHLY-LINEAR, CURRENT-FEEDBACK RESISTIVE SOURCE-DEGENERATED MOS TRANSCONDUCTOR

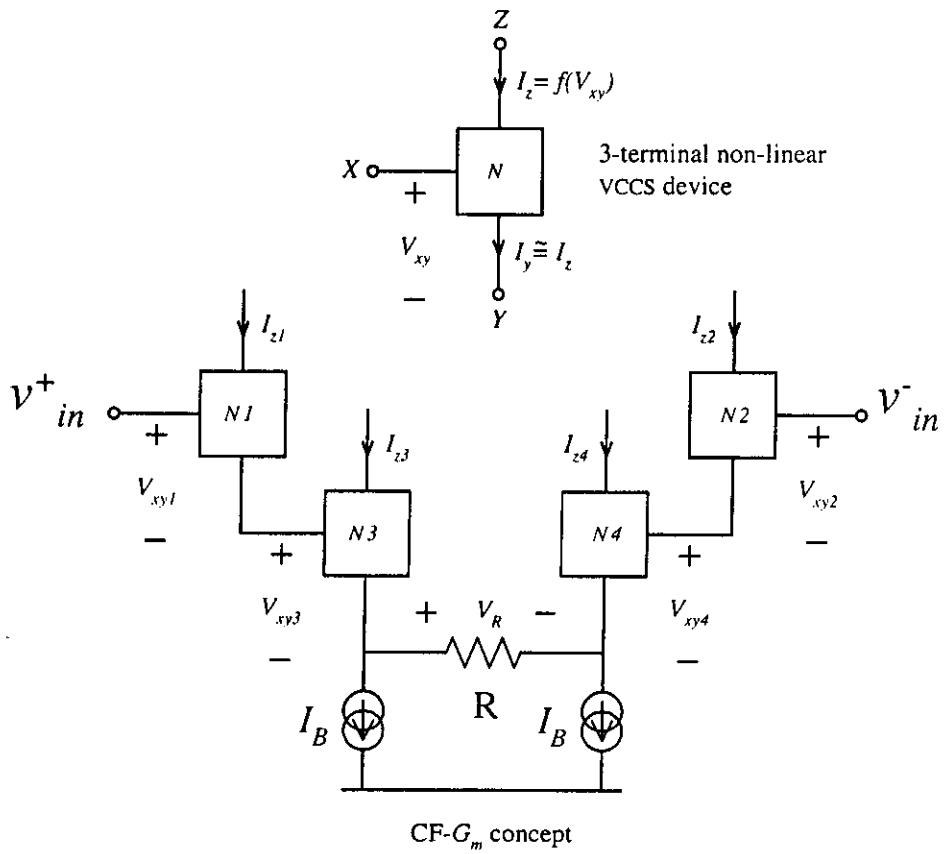
1.1 INTRODUCTION

Transconductors or voltage-to-current converters G_m are fundamental building blocks in analog circuit applications ranging from wideband amplifiers, high-frequency continuous-time filters, high-speed continuous-time delta sigma A/D converters, and other interface circuits. In many of these applications, highly-linear and large dynamic range transconductors are essential because they usually determine overall performance of the whole circuits and systems. Numerous circuit techniques have been proposed to improve the linearity performance of the transconductor [1.1]-[1.6] and, interestingly, they all can be classified as variants of the classical source-degeneration technique using passive resistors. These resistive source degeneration transconductors can be further divided into two main categories, namely (a) those based on the 'super G_m' arrangement in which a negative *voltage* feedback loop formed by a high-gain voltage amplifier [1.1]-[1.3] and (b) those based upon device's non-linearity cancellation by utilizing positive *current* feedback [1.4]-[1.6]. In this literature, a compact, highly-linear resistive CMOS source-degeneration transconductor based upon an alternative current-feedback (CF) structure will be presented. Unlike many previously reported linear resistor based transconductors, the proposed G_m's require only a small number of extra transistors, and therefore the circuit complexity and power consumption are kept at minimum. Comparison between the conventional G_m and the proposed circuits is provided via simulated performances.

1.2 PRICIPLE OF CURRENT-FEEDBACK SOURCE-DEGENERATED TRANSCONDUCTOR

There are number of previously proposed transconductors which can be considered as a current-feedback resistive emitter/source-degenerated type [1.4]-[1.6]. The Caprio's Quad [1.4] can be viewed as the circuit which has been developed from the translinear principle [1.7]. These G_m's employ the same technique of generating equal but opposite voltage variations to counterbalance transistor's

non-idealities resulting in a perfect voltage-to-current conversion by the source-degenerated resistor. The general principle of this current-feedback non-linearity compensated transconductor can be explained by considering the circuit diagram in Fig.1.1. Each rectangular block represents a three-terminal *non-linear* voltage-controlled current source, for example, it could be either BJT or MOS transistor. By assuming that the relationship between current I_z (= I_y) and voltage V_{xy} can be expressed by a non-linear function $f(\cdot)$ such that



CF-G_m concept

Fig.1.1 Conceptual structure of a current-feedback resistive source-degenerated transconductor

$$I_z = f(V_{xy}) = I_S \exp(V_{xy} / V_T) \tag{1.1}$$

for a collector current of BJT operating in a forward-active mode with V_{xy} = V_{be} being a base-emitter voltage, and

$$I_z = f(V_{xy}) = \frac{\mu C_{ox}}{2} \frac{W}{L} \left(V_{xy} - V_{TH}\right)^2 \tag{1.2}$$

for a drain current of MOS operating in a saturation region with $V_{xy} = V_{gs}$ being a gate-source voltage. By using KVL, the input voltage can be written as

$$\begin{aligned} V_{in} &= V_{xy1} + V_{xy3} - V_{xy4} - V_{xy2} + V_R \\ &= f^{-1}(I_{z1}) + f^{-1}(I_{z3}) - f^{-1}(I_{z4}) - f^{-1}(I_{z2}) + V_R \end{aligned} \tag{1.3}$$

It is therefore necessary to eliminate the device's non-linear inverse functions so that the input voltage is linearly transferred to appear across the degenerated resistor R, i.e., $V_{in} = V_R$. This can easily be accomplished by setting $I_{z1} = I_{z4}$ and $I_{z2} = I_{z3}$ which can be achieved by injecting feedback currents I_{z4} and I_{z3} into Y nodes of devices $N1$ and $N2$ respectively. Moreover, if the circuit is a fully balanced structure, the current signal swing of I_{z1} (= I_{z4}) will be equal but in an opposite direction to I_{z2} (= I_{z3}), e.g., $I_{z1} = I_B - i_{out}$, $I_{z2} = I_B + i_{out}$, we would have $V_{in} = V_R = R \cdot i_{out}$ or $i_{out} = V_{in}/R$ which is a perfectly linear V-to-I converter, i.e., a linear transconductor with transconductance (g_m) of $1/R$. In practice, the required feedback current can be provided by means of either cross-coupling [1.4] or current mirroring [1.5], [1.6].

1.3 Proposed Current-Feedback Source-Degenerated Transconductors

The current-feedback technique of Caprio's structure can be directly transferred to CMOS implementation as shown in Fig.1.2. Instead of employing current mirrors to provide current feedback as in the case of the transconductors proposed in [1.5] and [1.6], the cross-coupling transistors MN3—MN4 are utilized to *immediately* provide necessary compensating feedback current. If all the transistors are perfectly matched, it will render a linear transconductor with a transconductance $g_m = 1/R_S$. Alternatively, if a minimum supply voltage is required, PMOS transistors can be employed to complement NMOS devices in a place of either the input pair or the cross-coupling. It is worth noting that for a greater headroom and enhanced linearity, the constant bias current sources are not employed [1.8], the bias current is thus set by the degenerated resistor R_S and the DC common-mode input voltage level. This bias current is adaptively altered according to transconductance value (g_m is tuned by adjusting R_S which consists of resistive networks with triode MOS [1.8]), i.e., smaller g_m means smaller bias current compared to the fixed current consumption in a constant bias current source case. The non-linear cancellation technique of the circuit in Fig.1.2 is particularly attractive because it makes use of only two additional transistors, thus help reducing circuit complexity and minimising silicon area. Furthermore it does not require any extra bias current (unlike G_m's in [1.5],

[1.6]) because the bias current of the cross-coupling transistors has been *reused* by the input transistor pair.

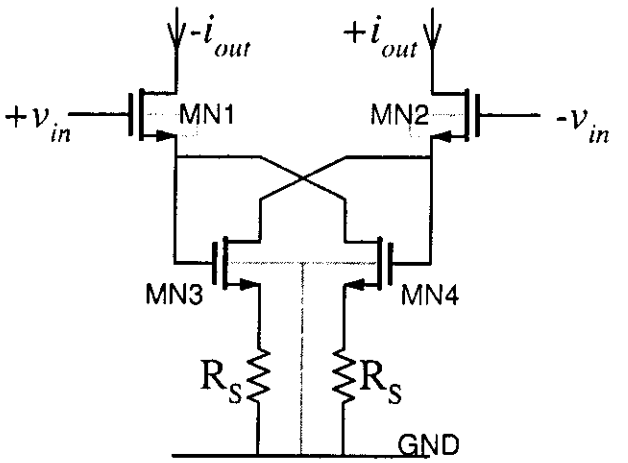


Fig.1.2 Current-feedback MOS transconductor with a cross-coupling for non-linearity compensation

The proposed transconductor in Fig.1.2 is designed in 0.35μm CMOS technology to have a nominal single-unit g_m value of 30μS (differentially) for an under-going analog baseband filter project. The aspect ratios W/L are 50μm/0.35μm same for MN1—MN4. At a typical operating point, the transconductor consumes 36μA under 3.0V supply with an input DC common-mode of 2.0V.

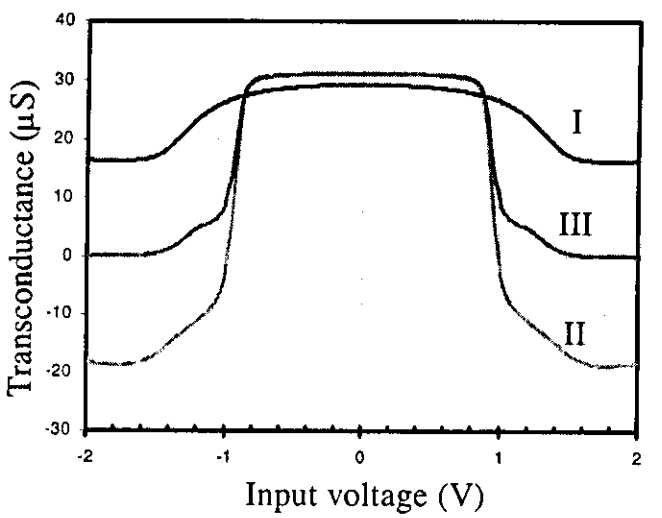


Fig.1.3 Transconductance curve of CF-G_m in Fig.1.2 (II) and Fig.1.4 compared with the conventional G_m (I) [1.8]

Simulations of the circuit have been performed via *Spectre*™. For a comparative performance demonstration, simulations of the conventional source-degenerate transconductor [1.8] were also

carried out. The DC-sweep characteristic of the circuit in Fig.1.2 is illustrated as curve II in Fig.1.3. For an input range of $\pm$0.8V, the current-feedback G_m renders a flatter response compared to a conventional G_m (curve I) [1.8], hence better linearity. However, it can clearly be seen from curve II that this G_m does inherit Caprio's quad's characteristics of limited voltage input range and inverted polarity of the transconductance. The input range is restricted because drains and gates of MN3 and MN4 are cross-connected making V_{DS} of these devices equipped with only one V_{GS} at zero-signal and consequently limit a signal swing head room. If V_{in} swing is too large, since MN1 and MN2 act as source followers, thus V_D of MN3 becomes very small and it would enter a triode operating region. Subsequently, current within MN3 and MN2 will be suddenly diminished and most of the output current will come out from MN1 and MN4, therefore the direction of output current (and transconductance) is inverted. This implies that in order to acquire a reasonably large input range, the cross-coupling transistors need to have large V_{GS}. One way to achieve this is by connecting bulk to ground if a relatively large *W/L* ratio has to be maintained. In order to keep a supply voltage low, source and bulk of the input transistors MN1, MN2 should be joined together (thus not applicable to single-well CMOS processes). In such case, there is an unavoidable V_{SB} mismatch between MN1 (MN2) and MN4 (MN3) and it inevitably degrades linearity of the transconductor because the non-linear terms in (1.3) are not completely eliminated. Therefore the body effect has to be taken into account and the MOS V-I relationship is altered to [1.9]

$$I_D = \frac{\mu C_{ox}}{2\alpha}\frac{W}{L}(V_G - V_{TH0} - \alpha V_S)^2 \qquad (1.4)$$

where V_{TH0} being the threshold voltage at zero source body voltage and the term α represents a body effect, ideally α = 1 for V_{SB} = 0. The *inverted* polarity of the transconductance due to devices entering triode operating region may cause instability when employing such transconductor in high-level filters. This problem can be elevated by adding another transistor pair MN5—MN6 to MN3—MN4 and then cross coupling their drain currents to combine with those from MN1—MN2 to produce the total output current resulting in another transconductor structure as depicted in Fig.1.4. In this way, the drain voltages of MN5—MN6 will not be severely affected by the input voltage. Unlike MN3—MN4, they will not enter triode operating region by a large excursion of V_{in} and their drain currents are not polarity inverted. Such characteristic will thus be combined with the transconductance generated from MN1—MN4 and produce an overall *single*-polar transconductance (non-negative).

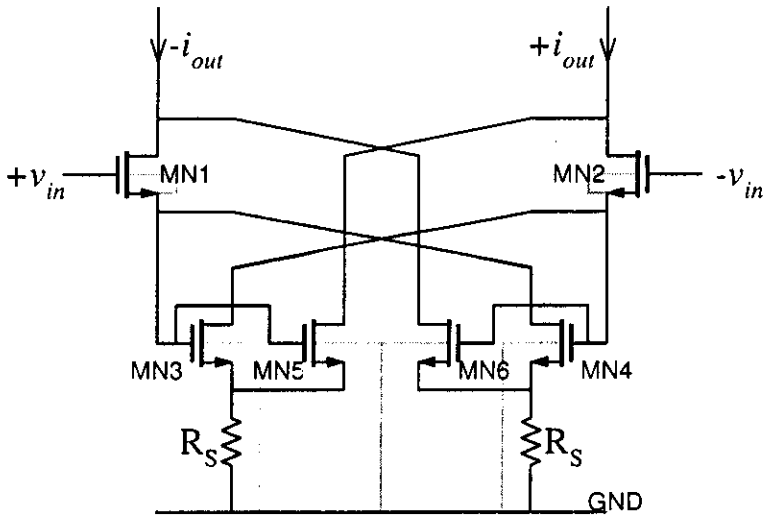


Fig.1.4 Single-polar current-feedback transconductor

The proposed G_m circuit of Fig.1.4 is designed with aspect ratios W/L of 50μm/0.35μm same for MN1—MN6. At a typical operating point (nominal g_m =30μS), the transconductor consumes 38μA under 3.0V supply with an input DC common-mode of 2.0V. Transconductance plotted against DC-sweep input voltage is also shown as curve III in Fig.1.3 where it can be clearly seen that no polarity inversion has occurred. Comparing with the g_m obtained from the ordinary structure presented in [1.8], it is obvious that this proposed circuit of Fig.1.4 also renders a flatter g_m response which signifies better linearity — similar to the performance obtained from the G_m of Fig.1.2. Again, the input range is about ±0.8V, which is more than sufficient for the application currently being investigated.

1.4 Simulation Results

More simulations of the proposed transconductors have been carried out. Fig.1.5 shows the transconductance of the circuit in Fig.1.4 for different source degeneration resistor R_s values ranging from 20kΩ (bottom) to 1kΩ (top). The input range has been slightly shrunk to ±0.75V for a small R_s =1kΩ. Furthermore current consumption for each transconductance value has been recorded and the transconductance/bias current efficiency is plotted in Fig.1.6. It is obvious that both proposed circuits of Fig.1.2 and Fig.1.4 render better g_m/I_{bias} efficiencies than those from the conventional G_m ([1.8]) for almost entire g_m range. Total harmonic distortions (THD) as a function of differential input amplitudes and frequencies are plotted in Fig. 1.7 and Fig.1.8 respectively for g_m =30μS. Evidently, the proposed transconductor renders a better THD performance by as much as 10dB over its the conventional G_m counterpart with an input amplitude up to 0.8V and with frequency range up to 1MHz.

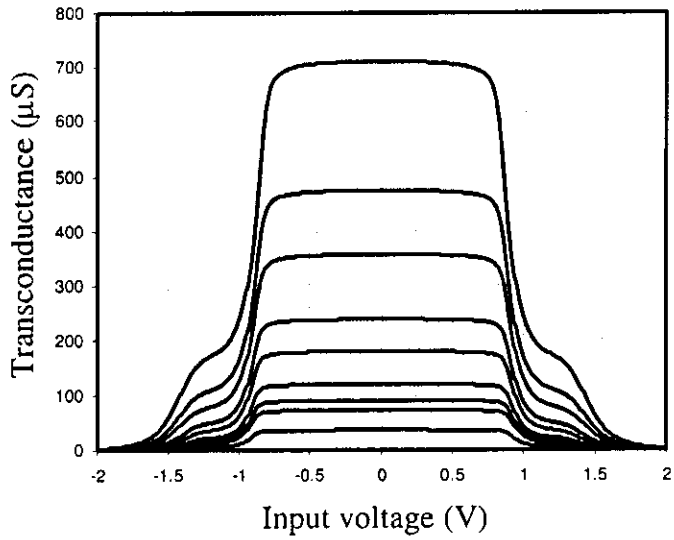


Fig.1.5 The simulated transconductance for different values of the source-degenerated resistor

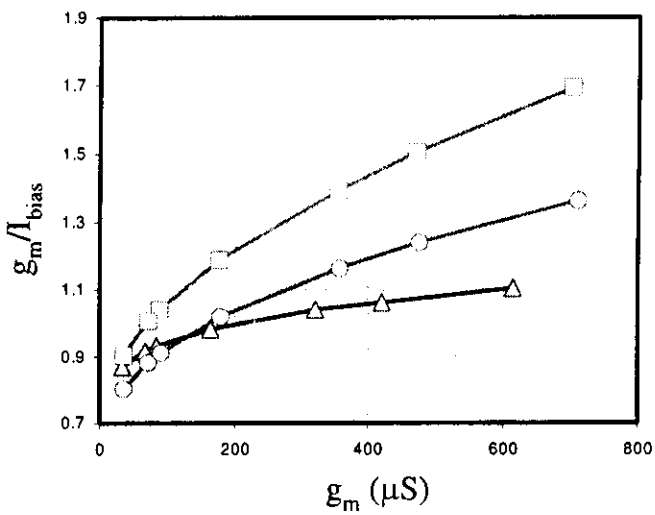


Fig.1.6 Transconductance/bias current efficiency: Δ conventional G_m [8], □ Fig.1.2, O Fig.1.4

1.5 CONCLUSION

A resistive source-degenerationCMOS transconductor with excellent linearity utilizing current-feedback has been described. The technique adds minimum complexity (just two or four additional transistors) to enhance linearity without extra current consumption, in other words high transconductance/current efficiency of an ordinary source degeneration transconductor is preserved

but with superior linearity performance. The transconductance's polarity inversion of Caprio's quad has also been solved by adding another cross-coupling transistor pair. The authors believe that it is possible to overcome V_{SB} mismatching problem by sizing the transistors with different W/L ratios similar to the technique presented in [1.6].

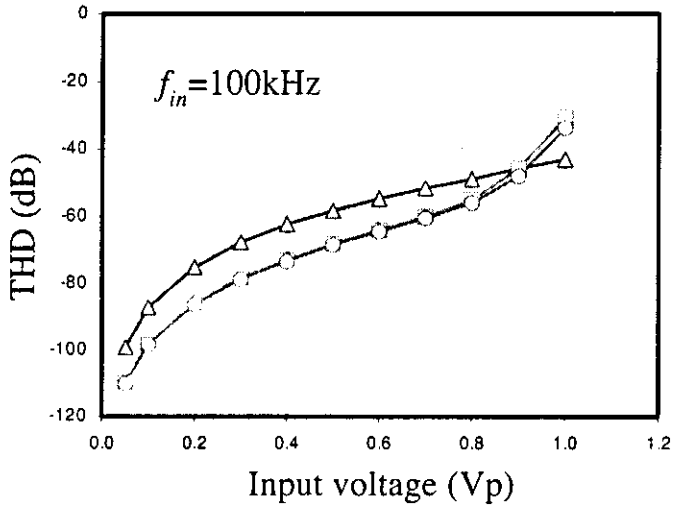


Fig.1.7 Simulated total harmonic distortion: Δ conventional G_m [8], □ Fig.1.2, O Fig.1.4

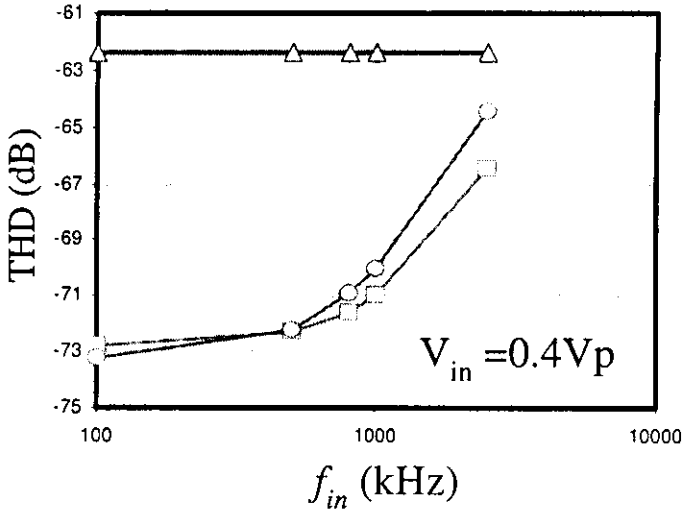


Fig.1.8 THD as a function of input frequency: Δ conventional G_m [8], □ Fig.1.2, O Fig.1.4

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CHAPTER 2

A 1.8-V CMOS POLYPHASE FILTER FOR DUAL-MODE BLUETOOTH/ZIGBEE TRANSCEIVER

2.1 INTRODUCTION

The low-intermediate frequency (low-IF) polyphase architecture has emerged as the preferred approach for achieving the required sensitivity in fully integrated wireless transceivers [2.1], [2.2]. Mainly driven by cost and power consumption, standard CMOS solutions for applications such as Bluetooth (IEEE 802.15.1) and ZigBee (IEEE 802.15.4) have set new challenges for circuit designers at both circuit and system levels. Bluetooth system has widely established itself in various well-known applications including wireless headsets, file sharing and printing, while ZigBee (also known as HomeRF Lite) is used for very simple wireless connectivity. The addition of ZigBee capability to a cell phone could enable the control of devices such as lights, electronic devices and central heating using the mobile handset. A dual-mode transceiver solution is being developed because in the price sensitive market for mobile devices, it is essential that this capability be added for minimal extra cost. Noting that coexistence issue of the two standards on the same frequency band is thoroughly discussed in IEEE Standard 802.15.4.

A polyphase filter or complex filter represents one of the key components in low-IF polyphase receiver. Owing to its asymmetric amplitude response, it has an ability to pass wanted channel signal while efficiently reject neighbouring channel interferers as well as unwanted image. A polyphase filter in this work is based upon transconductor-capacitor structure because of its simplicity, tuneability, linearity and high-frequency performance. The transconductor core circuit follows a linear, wide-tuning, low-noise and compact source degeneration type from [2.3] where the common-mode feedback and dc gain enhancement has employed a single network according to the topology originally proposed in [2.4].

2.2 REVIEW OF COMPLEX FILTERS

Fig.2.1 shows the basic principle of the complex filter. Starting with a real low-pass filter, the transformation $s \rightarrow s - j\omega_0$ is applied. This shifts the poles up the imaginary axis by ω_0 and transforms the lowpass response into an equivalent bandpass response centred at $\omega = \omega_0$. The transformation preserves both amplitude and phase characteristics and produces the required feature of having no image response at negative frequency. Synthesis of complex filters follows similar procedures to those for real filters except that it makes use of complex integrators. Fig.2.2 shows transformation from real to complex integrators implemented in the G_m-C technique. The transfer characteristic of the complex integrator in Fig.2.2 (b) is described by,

$$H(s) = \frac{i_{out}(s)}{i_{in}(s)} = \frac{G}{(s - j\omega_0)C} \tag{2.1}$$

where ω_0 is frequency shift given by $\omega_0 = G_0/C$. This demonstrates that the transformation $s \rightarrow s - j\omega_0$ is being performed as required.

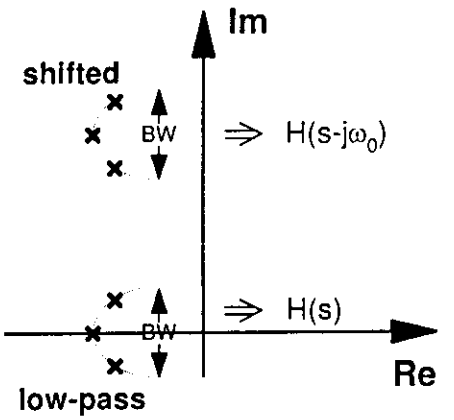

Fig.2.1: *Complex filter basics*

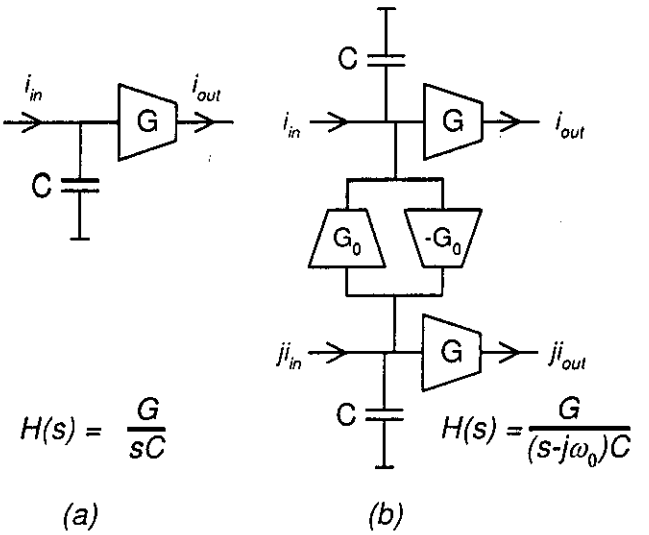

Fig.2.2: *Current-mode G_m-C integrator (a) real (b) complex*

2.3 TRANSCONDUCTOR CIRCUIT

The variable wide-band resistor source-degeneration transconductor proposed in [2.3] possesses many advantages including good linearity, low-noise, high frequency capability and low supply voltage. However, such structure inherits a couple of weak points that need special attention. This type of transconductor structure is prone to common-mode instability when employed for filter realisation. It is thus necessary to deploy a common-mode feedback loop comprising common-mode voltage sensing and error amplifiers. Moreover a low dc gain of the transconductor necessitates an additional negative conductance network to provide sufficient dc gain in order to achieve a required filter's frequency response.

As depicted in Fig.2.3, instead of using two separate networks to enhance common-mode stability and dc gain, a single network (MN3-MN6) adopted from the topology presented in [2.4] is employed. Its main feature is to ensure common-mode stability where the network forms a low impedance load for common signals and a high impedance load from differential signals, effectively resulting in common-mode stability. The technique has been successfully demonstrated with G_mC filters based on an inverter-type transconductor [2.5]-[2.9]. The second important feature is to help increase dc-gain of the transconductor. And this can be simply achieved by sizing transistors so that a positive feedback current from MN5—MN6 is higher than the negative feedback from MN3—MN4. Two-in-one

functionality thus allows additional devices to be kept at minimum; hence this helps save extra silicon area and power consumption.

The transconductor in Fig.2.3 possesses a nominal transconductance value of 20μS (V_{F3}=0.7V). Note that simple cascode PMOS current sources are employed to supply bias currents to the transconductor. The transconductor also deploys a tuning technique from [2.3]. Five tuning steps are required in this case to ensure a transconductance continuous sweep of $\pm$50% from the nominal value; each tuning voltage can be varied between 0.6V and 1.8V to adjust degeneration NMOS triode resistance.

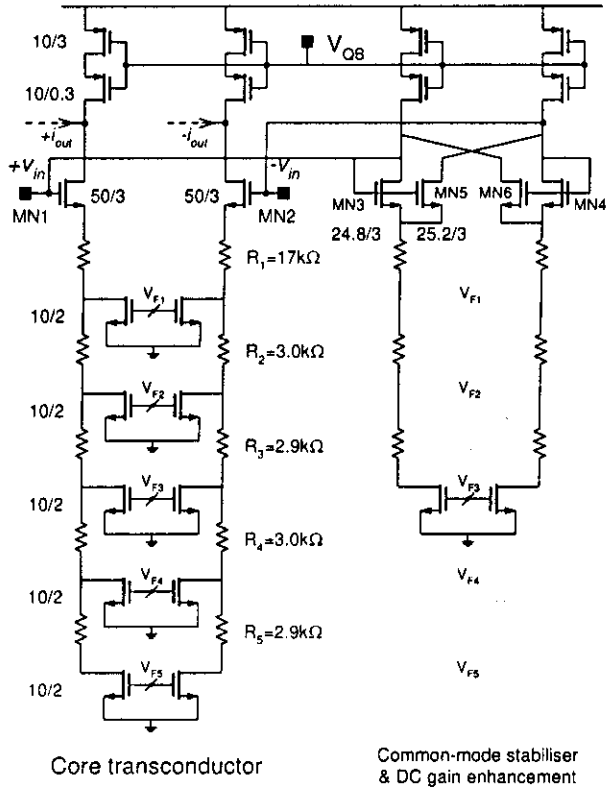

Fig.2.3: *Transconductor with common-mode stabilizer and dc gain enhancement*

At any time, only one pair of these degeneration NMOS's is on and the one-side degeneration resistance R_{di} is (only one V_{Fi} is on)

$$R_{di} \approx \underbrace{\mu_n C_{ox}\left(\frac{W}{L}\right)_i \left(V_{Fi} - V_{th}\right)}_{\text{triode-MOS resistance}} + \underbrace{\sum_{n=1}^{i} R_n}_{\text{ladder resistance}} \qquad (2.2)$$

where μ_n, C_{ox} and V_{th} are conventional parameters for NMOS transistor and the differential transconductance is approximately equal to $1/R_{di}$. To ensure a continuous transconductance sweep, the ladder resistors have to be designed according to (2.2) so that the adjacent tuning steps have adequate transconductance overlapping at their tuning boundaries when V_{Fi} is switched from one step to another. Because of a limited maximum available tuning voltage of 1.8V, a wide triode resistance variation can be achieved by employing a low threshold voltage NMOS device (V_{th}~0.4V) available in the technology as a tuning triode-MOS resistor. However, it is typical to have large V_{th} for the core transconductor MOS, MN1-MN2. This is because it normally happens that drain and gate voltages swings in opposite directions (sometimes with the same magnitude) from the same quiescent voltage (due to filter's cascade and feedback structure) and having a large V_{th} device will help maintain the transistors in saturation for large signal swing. Note that some of the transistors and resistors within the common-mode stabiliser (drawn in the light shade) can be omitted to save chip area without severely disturbing the circuit operation. It has only been included in Fig.2.3 to imitate the core transconductor structure.

Compare this transconductor to the class-AB inverter-type MOS transconductor employed for a dual-mode polyphase filter in [2.7]-[2.9], the proposed transconductor is inherently insensitive to supply voltage variation and it operates in a class-A manner.

2.4 FILTER DESIGN

A 5th-order 0.5dB equiripple Chebyshev complex filter depicted in Fig.2.4 is chosen for this work [2.7]-[2.9]. The design values for ZigBee and Bluetooth responses are given in Table 2.1. Notice that the design values are half of those used in [2.7]-[2.9] in order to minimise power consumption not higher than 2.5mW (this moderate power consumption has also been achieved by the 5th-order polyphase filter in [2.9]).

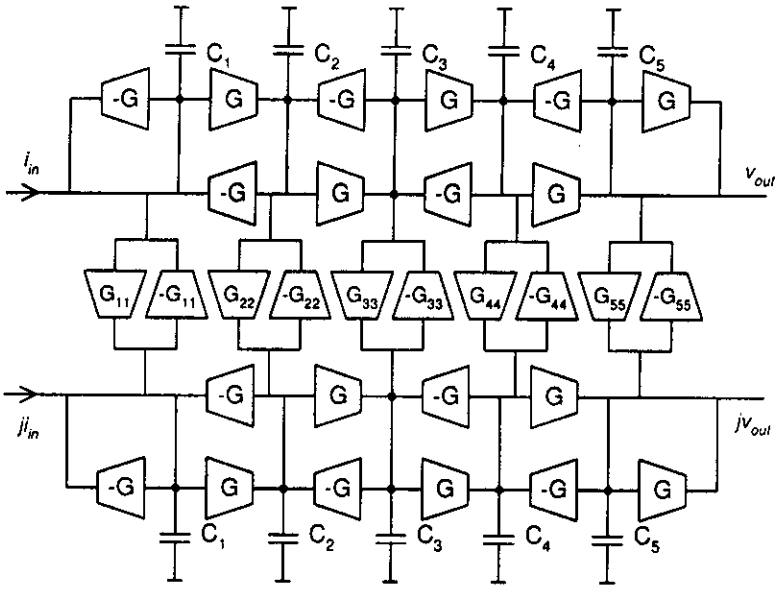

Fig.2.4: *Channel filter architecture*

Table 2. 1: *Design values for dual-mode filter*

Parameters	Bluetooth	ZigBee
G	20μS	20μS
G_{11}	56.86μS	56.86μS
G_{22}	41.99μS	41.99μS
G_{33}	84.70μS	84.70μS
G_{44}	40.99μS	40.99μS
G_{55}	56.86μS	56.86μS
C_1	9.05pF	4.53pF
C_2	6.53pF	3.27pF
C_3	13.48pF	6.74pF
C_4	6.53pF	3.27pF
C_5	9.05pF	4.53pF

A single feedback loop circuit shown in Fig.2.5 sets quiescent voltage V_{QB} for all transconductors within the filter. The diode-connected MOS (W/L=50μm/3μm) emulates the fact that under a quiescent condition, transistors MN3, MN5 and MN4, MN6 within the common-mode reject network in Fig.2.3 resemble a diode-connected NMOS. In this design the quiescent voltage is set to be at 1V. It should be also noted that the op-amp employed in Fig.2.5 is not required to be high performance; hence it can be easily designed under 1.8-V supply.

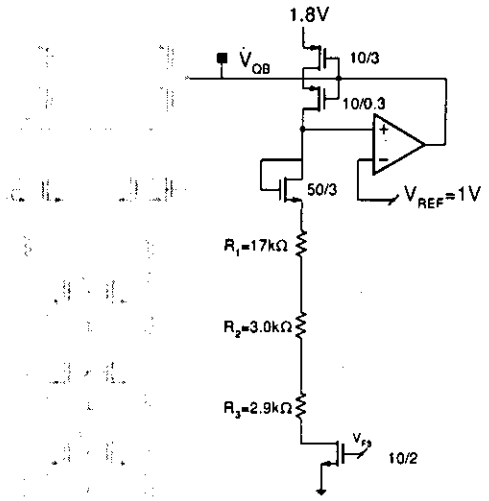

Fig.2.5: *Quiescent voltage setting-up circuitry*

2.5 SIMULATION RESULTS

All the simulations have been carried out using Spectre with Cadence design suite. Simulated frequency response of the complex filter employing 3.3-V 0.18μm digital CMOS process is shown in Fig.2.6-Fig.2.8. It can be seen that the simulated responses are very close to ideal. Note that the actual capacitor values have been trimmed according to the method described in [2.8] to take parasitic capacitance into account. Fig.2.6 shows two modes of operation (Bluetooth and ZigBee), obtained by switching the values of capacitor with the common set of transconductors. Fig.2.7 illustrates frequency tuning at nominal and two extremes by adjusting tuning voltage. This center frequency tuning capability of > 80% is more than enough to encounter process and temperature variations.

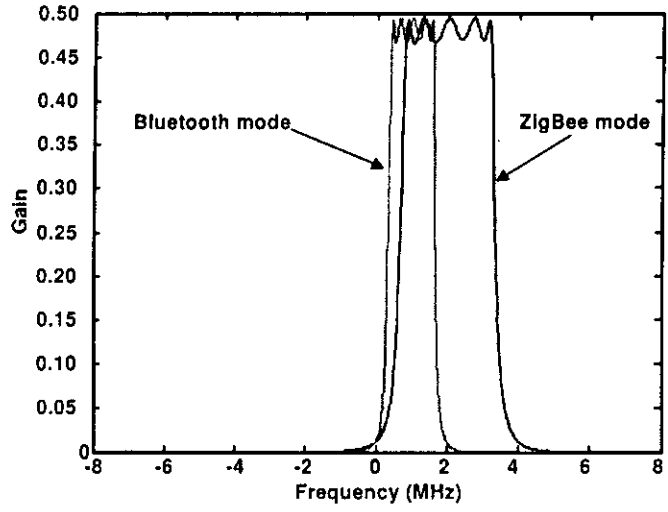

Fig.2.6: *Filter mode switching*

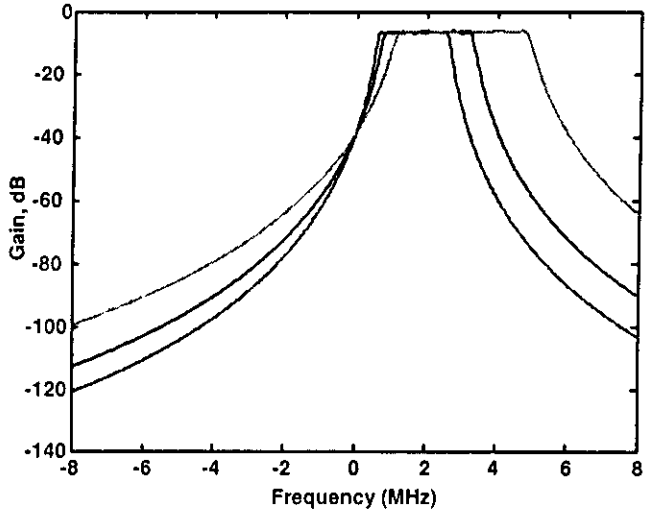

Fig.2.7: *Frequency tuning in ZigBee mode*

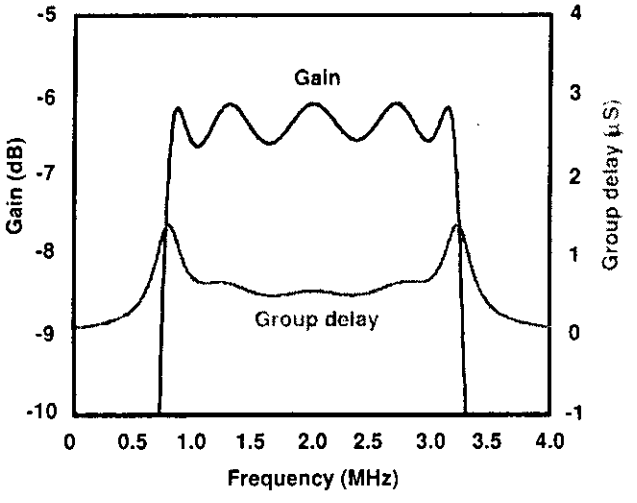

Fig.2.8: *ZigBee's passband response*

The filter common-mode rejection ability has been investigated by measuring common-mode signal frequency response and compare with differential signal as show in Fig.2.9. It can be seen that although the structure of Fig.2.3 does not reject common-mode signal *locally*, but globally the filter does have ability to suppress common-mode signals. The filter has also been subjected to a transient common-mode step response stability test [2.3], and the results guarantee its unconditional stability as illustrated in Fig.2.10.

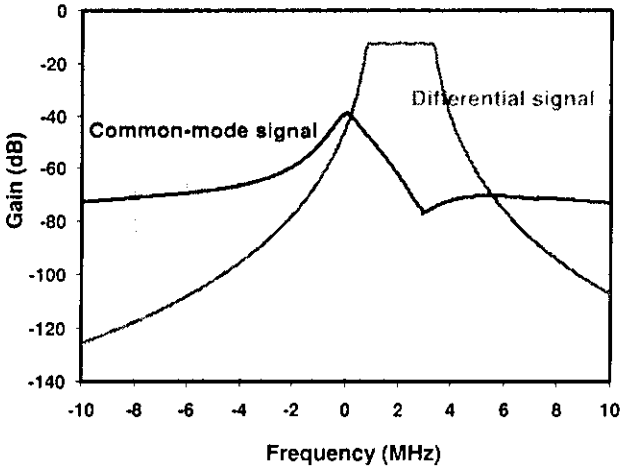

Fig.2.9: *Filter's frequency response: differential vs common-mode (single-end output)*

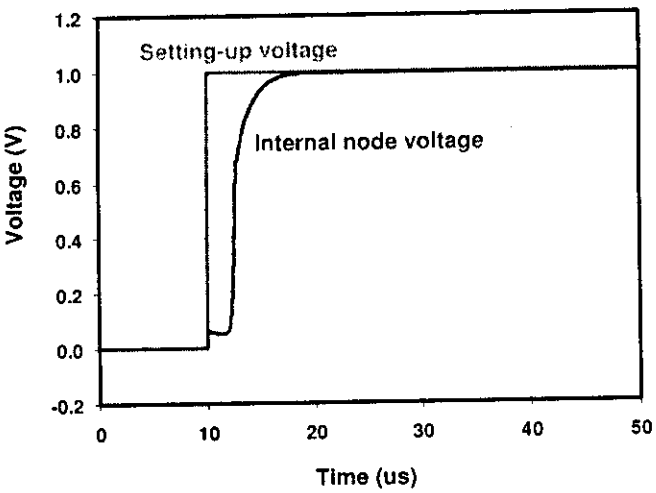

Fig.2.10: *Stability test with step response*

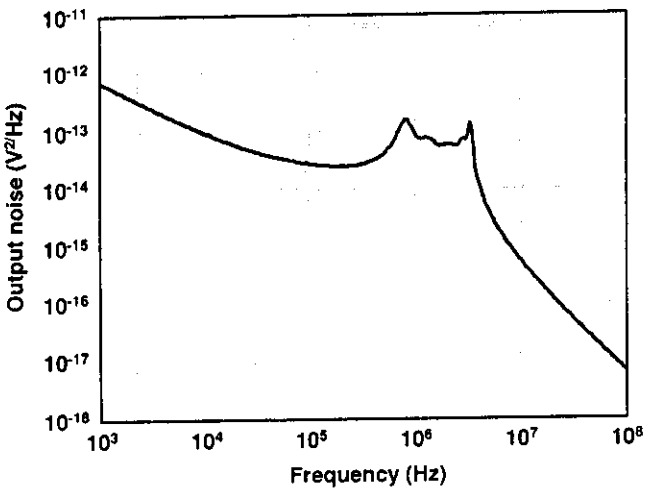

Fig.2.11: *Noise response (ZigBee mode)*

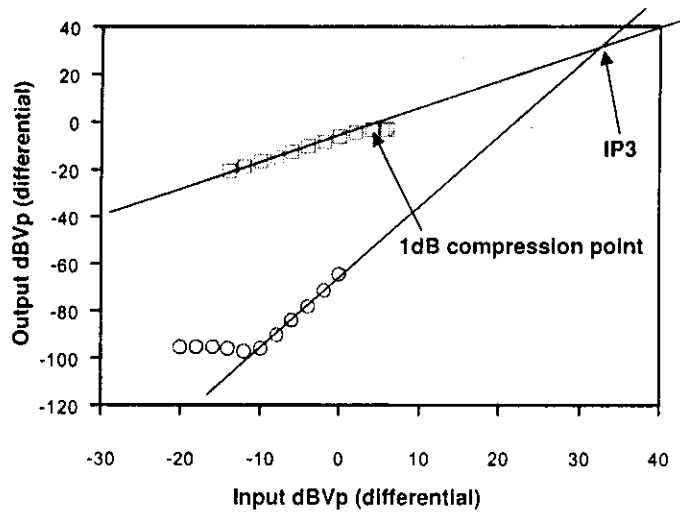

Fig.2.12: *Third-order intermodulation*

The ZigBee output differential noise is shown in Fig.2.11 where the total output noise integrated over the 100MHz bandwidth renders output noise power voltage of $2.5\times10^{-7}V^2$. The ZigBee signal compression characteristic of ZigBee-mode filter is shown in Fig.2.12 and it demonstrates a linear gain up to an input amplitude of 1Vp (0dBVp) differential and an input referred 1-dB compression point of 1.59Vp (or 4.03dBVp) differential (with corresponding output voltage of 0.68Vp). The signal-to-noise ratio is thus found to be 62.3dB.

The in-band spurious free dynamic range (SFDR), where the inter-modulation product has the same power as the filter noise, is found to be 51.3dB and 53.4dB for ZigBee and Bluetooth modes respectively. Out-of-band intermodulation of the distant blockers was also simulated as also shown in Fig.2.12 for ZigBee case (input tones at 6MHz and 10MHz for ZigBee and 3MHz and 5MHz for Bluetooth). It shows the ZigBee third-order intermodulation characteristic indicating an input referred third-order intercept point (IIP3) of 33dBVp differential with corresponding out-of-band SFDR of 59.6dB. The whole filter draws a total current of 1.38mA from a single 1.8-V supply. The overall performance for both modes is summarised in Table 2.2.

2.6 CONCLUSION

A 1.8V CMOS dual-mode fifth-order polyphase G_mC filter for Bluetooth/ZigBee transceiver has been designed. The complex bandpass filter is based on Gm-C filter structure with appropriate crossing transconductors to shift lowpass response to the required IF frequencies. It deploys a simple

source degeneration transconductor integrated with a network, which could simultaneously provide common-mode stability and dc gain enhancement.

Table 2.2: *Summarised filer performance*

Filter Response	Chebyshev	
Filter Order	5+5	
Filter ripple	0.5dB	
Supply voltage	1.8V	
Process	3.3V, 0.18μmCMOS	
Supply current	1.38mA	
Mode	Bluetooth	ZigBee
Centre Frequency	1MHz	2MHz
Bandwidth	1.2MHz	2.4MHz
Gain	-6.18dB	-6.18dB
Output noise	$1.4\times10^{-7}V^2$	$2.5\times10^{-7}V^2$
Input 1dB Comp.	1.59Vp	1.59Vp
Signal/Noise (SNR)	64.9dB	62.3dB
IIP3 (distant blocker)	36.4dBVp	33dBVp
SFDR		
(a) Distant blocker	62.1dB	59.6dB
(b) In-band	53.4dB	51.3dB

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CHAPTER 3

APPLICATION OF REVERSE-ACTIVE *NPN*S FOR COMPACT, WIDE-TUNING F_T-INTEGRATION-BASED FILTERS IN SIGE HBT BICMOS TECHNOLOGY

3.1. INTRODUCTION

The rapid growth of today's wireless multi-gigabit communication market has placed an ever increasing demand on integrated filter performance particularly in terms of very high operating frequencies with acceptable dynamic range and low power consumption. Among conventional active filtering techniques such as G_m—C and log—domain filters, f_T—integration technique has portrayed itself as a viable alternative for very high frequency applications [3.1]-[3.4].

A mature SiGe HBT BiCMOS technology is an excellent match for realisation of cost-effective, highly integrated high-speed data communication and wide-bandwidth digital wireless architectures at microwave frequencies. This is because high performance analog circuitry (provided by heterojunction bipolar transistor —HBT) can co-exist with sophisticated digital blocks (CMOS). Bandgap engineering enables process designers to achieve a SiGe HBT with all-around superior performances compared to a conventional Si BJT device [3.5]-[3.8].

This work demonstrates the feasibility in applying HBT devices in SiGe BiCMOS technology to f_T—integration technique. Specifically, the HBT's will be employed to implement a low-voltage, wide-tuning 5-GHz f_T—integration-based bandpass filter. It will be shown that a large frequency tuning range at microwave operating frequencies is accomplished in the SiGe filter via the existing structure using lateral *pnp*'s as large base transit time tuning devices. The improved structure using reversed active vertical *npn*'s with a significant reduction in chip area is proposed.

3.2. f_T-INTEGRATION PRINCIPLE

f_T—integration technique has been thoroughly discussed in previous literatures [3.1]-[3.4] and only a brief overview of the principle is addressed here for better circuit understanding in subsequent sections.

Base charging dynamic of a bipolar junction transistor results in a charge control equation which relates *large-signal* base current I_b and collector current I_c as

$$I_b = \tau_b \frac{dI_c}{dt} + \frac{I_c}{\beta_0} \tag{3.1}$$

where τ_b is the transit time in the base. This mathematical function of integration lies as a basis of f_T—integration. The operation of SiGe *heterojunction* bipolar junction transistor (HBT) is also governed by the base charging dynamic similar to the conventional homojunction BJT. Therefore it is conceptually feasible to apply f_T—integration technique to HBT's for filter implementation.

3.3. WIDE-TUNING f_T-INTEGRATOR DESIGN IN SiGe HBT BiCMOS TECHNOLOGY

Based upon the f_T—integration principle presented in the previous section, the first version of the f_T—integrator designed within SiGe HBT 0.8μm BiCMOS process is shown in Fig.3.1 which has been migrated from the low-voltage f_T—integrator presented in [3.4]. Four lateral *pnp*'s Q_F connected in parallel have been used on each side of the integrator in order to achieve the required nominal operating frequency of 5GHz and wide frequency tuning range. Note that the lateral *pnp* symbol has an extra node indicating a gate terminal which always has to tied to the most positive supply. This is because this lateral *pnp* is simply constructed from the existing PMOS structure, its gate thus has to be biased positively so that channel inversion never occurs.

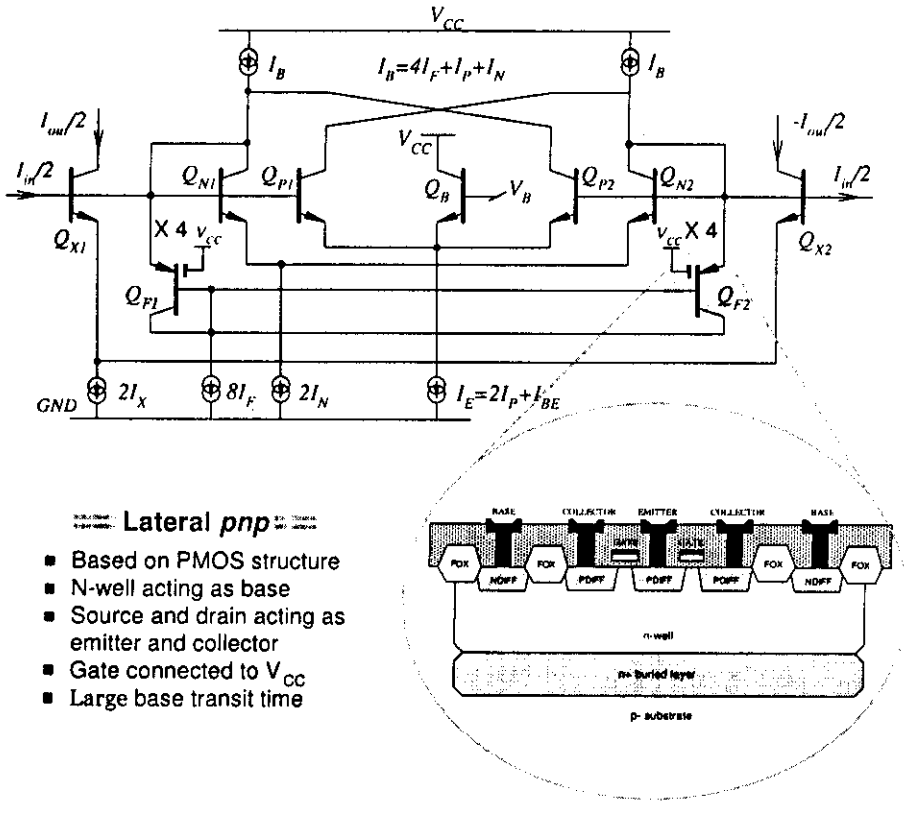


Fig.3.1: *f_T-integrator in SiGe BiCMOS with lateral pnp as tuning device (migrated from[3.4])*

The unity-gain frequency f_U of the f_T—integrator presented in Fig.3.1 can be expressed as

$$f_U = \frac{1}{2\pi\tau_b\left\{1+m\frac{\tau_{bf}}{\tau_b}\frac{I_F}{I_X}+\frac{I_P}{I_X}+\frac{I_N}{I_X}\right\}} \tag{3.2}$$

where τ_b is the base transit time of the forward-active *npn* and τ_{bf} is that of the frequency-tuning device Q_F with m being the number of Q_F in parallel. Since typical values for I_P and I_N are negligibly small compared to I_X and I_F, the tuning range can be estimated from (3.2) to be

$$\frac{f_{U_{max}}}{f_{U_{min}}} \approx \frac{f_U\big|_{@\,I_F=0}}{f_U\big|_{@\,I_F=I_{F\,max}}} = 1+m\frac{\tau_{bf}}{\tau_b}\frac{I_{F\,max}}{I_X} = 1+m\frac{\tau_{bf}}{\tau_b}\frac{p\cdot I_{F0}}{I_X} \tag{3.3}$$

where m=4 in Fig.3.1. I_{Fmax} is the maximum possible frequency-tuning current which may be written as $I_{Fmax}=p\cdot I_{F0}$, where p is the ratio of the maximum possible I_F relative to the nominal bias value I_{F0}. Normally the ratio p is the same for any type of HBT or BJT. Equation (3.3) suggests that the term on the right hand side has to be large in order to achieve a wide tuning range. An advantage in utilizing

lateral *pnp*, commonly available in standard BiCMOS process, for Q_F is a considerable tuning range improvement while keeping power consumption at minimum. That is, only a small *m* is required to accomplish a large tuning range, owing to the *pnp* 's inherently large base transit time. Moreover, the lateral *pnp* normally requires low bias current I_{F0}. In other words, with lateral *pnp*, the second term in (3.3) can be made large without sacrificing excessive extra current consumption. Small nominal bias current also helps minimise collector and base shot noise.

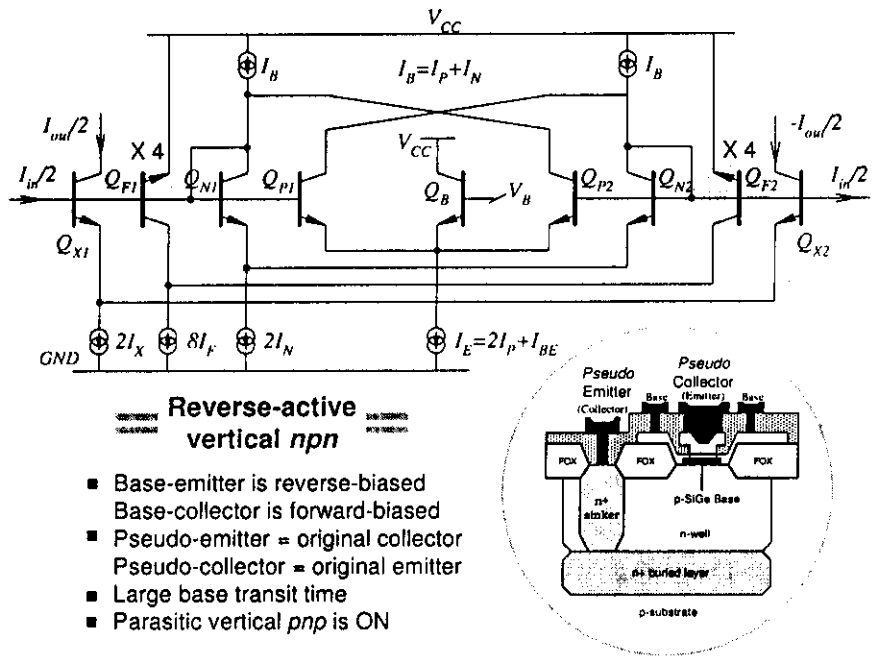


Fig.3.2: *The proposed f_T-integrator with vertical reverse-active npn as frequency tuning device*

However, the employment of lateral *pnp* results in one major disadvantage of occupying huge silicon area and so this might not be an ultimate solution for tuning range extension. It would be ideal if there is a more compact device but with an inherently large base transit time and low nominal bias current in a similar order to that of the lateral *pnp*. Our proposal is to employ a vertical *npn* operating in a reverse-active region, i.e., with the reverse biased base-emitter and forward biased base-collector junctions. Because of its asymmetry (both in doping profile and physical structure, see Fig.3.2), a reverse-active *npn* possesses an inferior characteristic compared to the forward-active mode. The large base transit time of a reverse-active *npn*, which is normally considered inferior, can be turned into an advantage by performing a significant role of frequency tuning range enhancement. In a typical BiCMOS, bipolar or SiGe BiCMOS process including the one employed in this work, it is found that lateral *pnp* and reverse-active *npn* possess a similar large value of $\tau_{bf} \cdot I_{F0}$, which means that these two

types of devices require the same number of transistors to obtain the same tuning range. Therefore with a benefit of saving chip area, there is no penalty on either current consumption or number of devices in replacing lateral *pnp* with a reverse-active vertical *npn*. In this way, we are able to extend f_T—integrator's frequency tuning range without sacrificing neither power consumption nor chip area by simply utilising *npn* operation in a region which has been widely regarded worthless.

The f_T—integrator structure employing a reverse-active vertical *npn* as frequency-tuning device is illustrated in Fig.3.2. Similar to the lateral *pnp* case, four reverse-active *npn* are employed on each side of the integrator in order to achieve a 5GHz nominal operating frequency. Both circuits in Fig.3.1 and Fig.3.2 use a supply voltage of $V_{BE} + 2V_D$, where V_D is the voltage drop across each current source and the typical supply voltage could be estimated to be 0.8 + 2(0.5) = 1.8V.

There are various issues that have to be taken care of when designing circuit using reverse-active vertical *npn*. Firstly, voltage across emitter-base junction has to be kept lower than a relatively low emitter-base breakdown voltage. The supply voltage of circuit in Fig.3.2 is thus restricted to a low value. If it is necessary to have a high supply voltage (e.g. 3V), the reverse-active *npn* Q_F in Fig.3.2 can be modified by disconnecting its emitter (pseudo collector) from V_{CC} and tying this to the base. In this way, the Q_F's has formed a diode-connected configuration and base-emitter breakdown damage can be avoided. Secondly, when operating the transistor in a reverse mode, the parasitic vertical *pnp* formed by base-collector-substrate structure is inevitably turned ON. Consequently, there will always be a small leakage current wasted into substrate.

3.4. SIMULATION RESULTS

The resonators based on the proposed integrators of Fig.3.1 and Fig.3.2 have been simulated with V_{CC}=1.8V using SpectreRF within Cadence design platform. The devices are taken directly from the library of the foundry's design kits of HBT SiGe 0.8μm BiCMOS process without any modification. A double-base *npn* occupies a total area of 60μm^2 (effective *emitter* area = 2μm×0.8μm) which is much smaller than 400μm^2 of lateral *pnp* (effective emitter area = 3.6μm×3.6μm). Therefore, in this particular technology, the reverse-active vertical *npn* occupies silicon area less than one-sixth of the lateral *pnp*'s area which significantly help optimise circuit compactness and reduce fabrication cost. For rough estimation, if a single vertical *npn* represents one unit chip area, it would mean that the proposed integrator of Fig.3.2 consumes only one-fourth of the area occupied by the integrator in Fig.3.1. Regarding device characteristics, the *npn* HBT has a peak f_T of 30GHz at bias collector

current = 750μA with corresponding β_0 of 80 and base resistance = 300Ω. In a reverse-active mode, the same device possesses a peak f_T= 800MHz with β_0 = 10 at collector current of 80μA. Comparing to a reverse-active *npn*, lateral *pnp* have a slightly superior device characteristic with peak f_T =3GHz at collector current of 90μA with the corresponding β_0 =20.

Simulation results show that the centre frequency (f_c) can be widely tuned from 1.9GHz to 6.7GHz by varying I_F from 600μA to 0.25μA while fixing I_X at 750μA as shown in Fig.3.3. Such a wide frequency tuning of over 300% is a solid confirmation of reverse-active *npn* and lateral *pnp*'s expected functionalities. Resonator frequency responses are illustrated in Fig.3.4 indicating centre-frequency (f_c) and quality factor (Q) tuning.

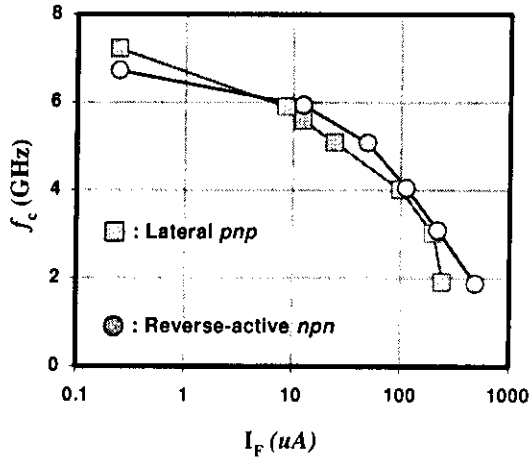
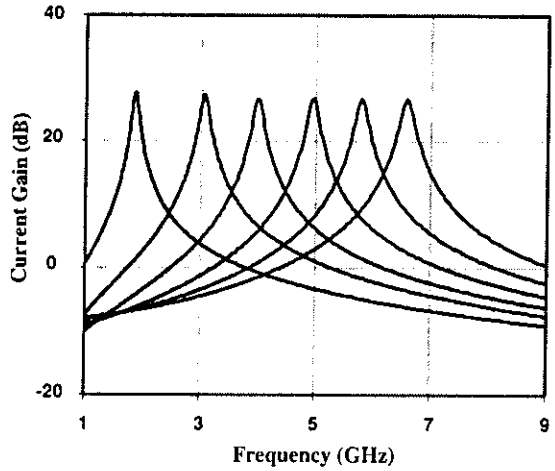
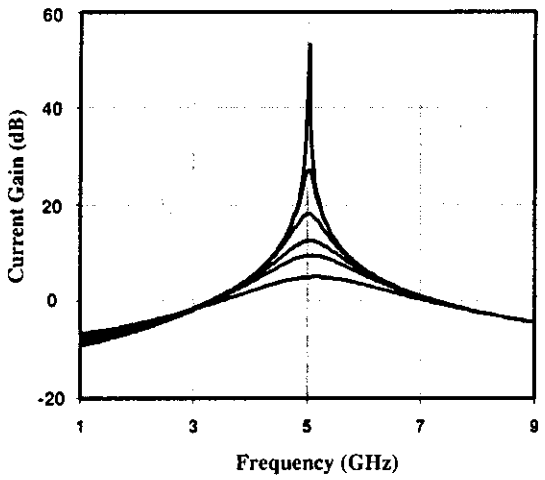


Fig.3.3: *Centre-frequency vs I_F*



(a) f_c tuning



(b) Q tuning

Fig.3.4: Frequency response (reverse-active)

The spurious-free dynamic range, SFDR (ratio between a wanted signal and an unwanted third-order intermodulation at the point where the third-order intermodulation power is equal to noise power) is plotted against centre frequencies is shown in Fig.3.5 for two values of Q = 5 and 10. Note that SFDR is simulated with input two-tone signals of 0.5% frequency separation and the noise power is measured by integrating ac-simulated noise within -3dB signal bandwidth. At nominal centre frequency of 5GHz, the SFDR's are found to be 30dB and 33dB for Q = 10 and 5 respectively.

Fig.3.6 illustrates how SFDR varies with Q for the proposed circuits at f_c=5GHz and they are compared with the prototype in Si BiCMOS at f_c =1GHz. It can be seen that the proposed SiGe circuits render SFDR similar to those reported in [3.4] but with an operating frequency higher by fivefold. A fair comparison of filter overall performance is normally obtained by means of a figure of merit (FoM) which is defined here as

$$\text{FoM} = \frac{f_c \times \text{SFDR}}{\text{Power consumption per pole}} \tag{3.4}$$

According to FoM definition, the filter with a better performance possesses a higher FoM. FoM comparisons are plotted against f_c in Fig.3.7 for Q = 10. It is clear that at the region around nominal operating frequencies, the proposed circuits (both with lateral *pnp* and reverse-active *npn* as a tuning device) give better FoM over the filter implemented in Si BiCMOS where an improvement by a factor as large as four can be observed.

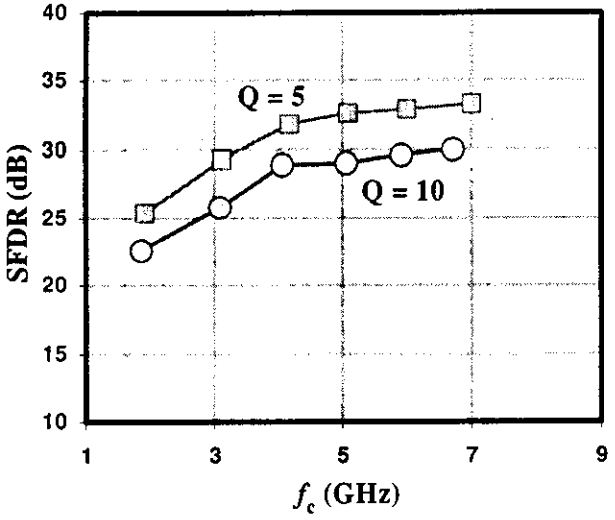


Fig.3.5: *SFDR vs f_c (reverse-active)*

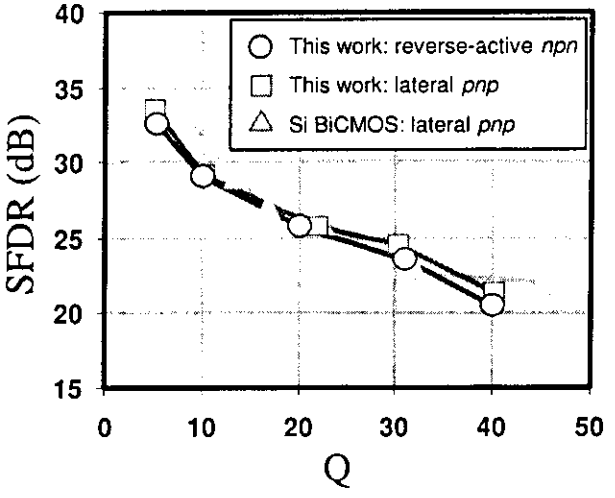


Fig.3.6: *SFDR vs Q (reverse-active)*

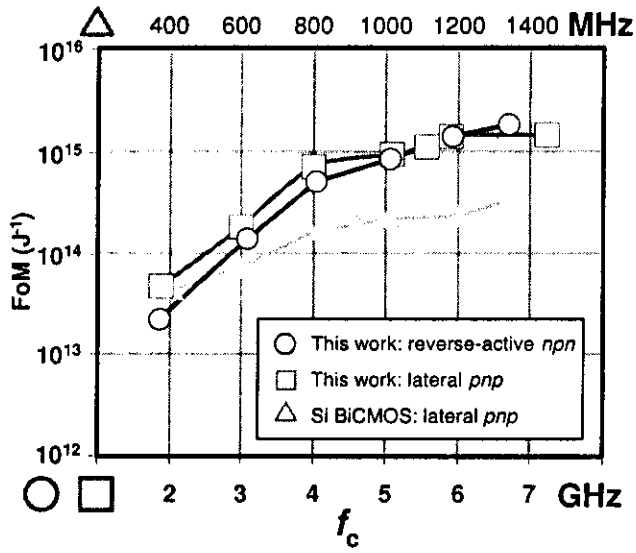


Fig.3.7: *Figure of merit comparison*

3.5. Conclusion

f_T—integration technique has been successfully demonstrated via simulations in HBT SiGe 0.8μm BiCMOS technology. Addition to existing technique in deployment of a lateral *pnp* for frequency tuning range enhancement, a reverse-active vertical *npn* has been proposed to achieve the same task while also keeping current consumption and chip area at minimum. The resonators can be widely tuned from about 2GHz to more than 6GHz, i.e., tuning range is greater than three-fold. At nominal, the resonators render SFDR of 30dB and 33dB for Q = 10 and 5, respectively. FoM comparison between the SiGe filters and the previous prototype implemented in Si enjoys improved performances as large as four times.

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CHAPTER 4

HIGH-GAIN CURRENT AMPLIFIERS FOR LOW-POWER MOSFET-C FILTERS

4.1 INTRODUCTION

The rapid growth of today's wireless communication market has placed an ever-increasing demand on integrated filter performance particularly in terms of linearity, dynamic range and low power consumption under a low voltage supply constraint. The MOSFET-C filter design technique has portrayed itself as a simple and effective method for integrating high complexity continuous-time filters on a single CMOS chip with large dynamic range and accurate frequency response [4.1]-[4.5] .

A key building block in MOSFET-C filters (and also as in a classical active-RC filter) is an operational amplifier (OA). However, it has been demonstrated in [4.1], [4.2] that an operational transconductance amplifier (OTA) —— typically consumes less power than OA, with sufficiently large transconductance, can also be employed as an active building block. Achieving a large transconductance OTA under a low voltage supply might not be straightforward. In the past decade, OTA have been extensively researched for various circuit applications [4.3]-[4.8]. This work employs a very high-gain current amplifier (CA) as an alternative to OA and OTA in MOSFET-C filter (active-RC) while still maintains a required filter realization. Previously, high-gain current amplifiers have also been used in voltage amplifier design ([4.9], [4.10], [4.11]) and recently in $g_m C$-Opamp high frequency filters ([4.12]) in order to give high-bandwidth and low-distortion performance.

4.2 MOSFET-C INTEGRATOR EMPLOYING CURRENT AMPLIFIER

Consider a MOSFET-C or active-RC integrator employing an ideal current amplifier (CA) with current gain of A_i as an active building block in Fig.4.1, a simple analysis yield voltage output/input relationship (in terms of admittance Y and A_i)

$$\frac{v_{out}}{v_{in}} = -\frac{Y_1}{Y_2 + \dfrac{Y_2 + Y_L}{A_i}} \tag{4.1}$$

where $Y_1=1/R$, $Y_2=sC$ and Y_L = load admittance. If $A_i >> Y_2 + Y_L$, an ideal integrator transfer function can be realised accordingly, that is

$$\frac{v_{out}}{v_{in}} = -\frac{Y_1}{Y_2} = -\frac{1}{sRC} \tag{4.2}$$

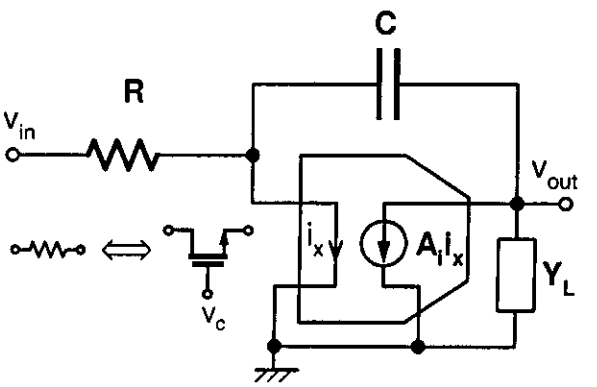


Fig.4.1 *MOSFET-C or active-RC integrators employing high-gain current amplifiers*

Similar to OA-RC and OTA-RC cases, because the current amplifier in Fig.4.1 is connected in a closed loop formation, therefore the current amplifier may be non-linear as long as high current gain is present, and no linearisation circuit is needed. Fig.4.2 shows a possible architecture of a very high-gain current amplifier. The high current gain of this current amplifier comes from an intermediate high-impedance node X and it is equals to $A_i = Z_x \cdot G_m$.

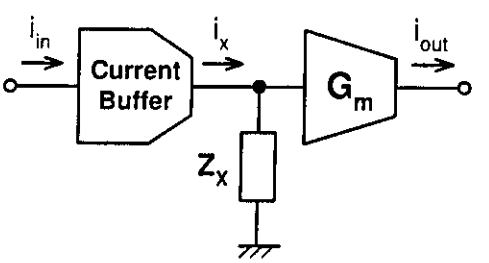


Fig.4.2 *High-gain current amplifier concept*

4.3 Proposed High-Gain Current Amplifiers for MOSFET-C or Active-RC Filters

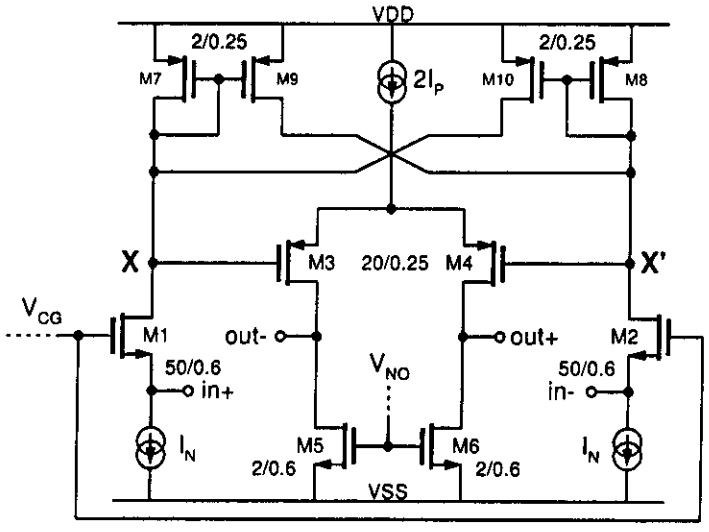
A balanced MOSFET-C integrator employing a high-gain current amplifier based upon the structure in Fig.4.2 is depicted in Fig.4.3a and Fig.4.3b. A common-gate NMOS structure M1-M2 is utilised as a current buffer allowing input current to flow into high impedance nodes X, X′. At these nodes in Fig.4.3a, a diode-connected PMOS (negative feedback, M7-M8) is combined with the cross-coupling PMOS (positive feedback, M9-M10) to realise high impedance. However, such high impedance is only recognised by differential signals. In contrast, these same nodes are seen by common-mode signals as low impedance, hence DC bias voltage can be established without requiring additional common-mode feedback (CMFB) amplifier as in case of the amplifier in [4.9]. This gain enhancement and DC voltage setting-up technique thus consumes no extra current consumption. An output stage of the amplifier utilises a PMOS source-coupled pair with current source $2I_P$ where it provides capability of common-mode rejection for the amplifier. However, such structure resembles class-A output configuration, therefore the output current swing is limited by a current source ($2I_P$).

A more attractive current amplifier structure is shown in Fig.4.3b where PMOS M3, M4 are connected in parallel to M11, M13 and M12, M14 respectively in order to provide output current in a class-AB manner allowing large current signal excursion because it is not limited by fixed current source. This circuit thus should render better linearity than its counterpart in Fig.4.3a. However, this output structure requires M5-M6 and current mirrors M7-M10 with an appropriate cross-coupling to provide (i) common-mode rejection (ii) differential signal addition (combining drain signal currents of M5 with M4 and M6 with M3). Fig.4.4 illustrates how this particular output stage handle signals differently. Such circuit arrangement provides feed-forward common-mode rejection, but in a different manner to that proposed in [4.13], because the *differential* signals (and transconductances) of M3, M6 and M4, M5 are added constructively. Therefore it can effectively provide common-mode rejecting without incurring any penalty in the overall transconductance/bias-current efficiency, i.e., bias current consumed by M5-M8 is not wasted just for common-mode rejection.

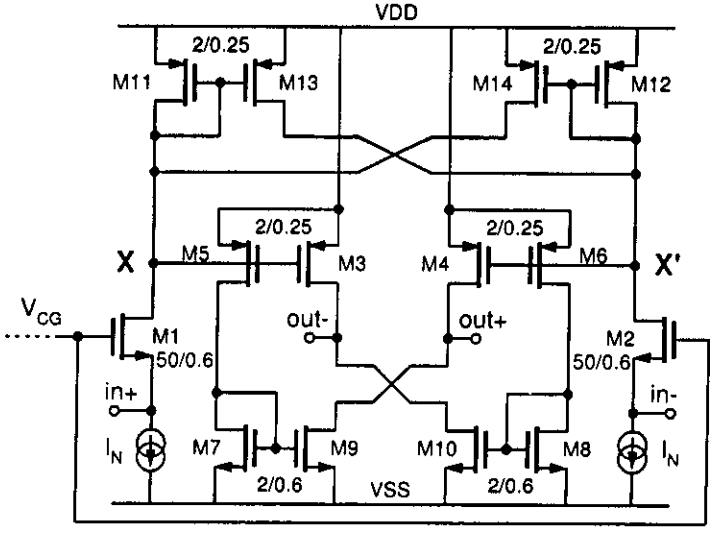
Additional simple tuneable positive or negative resistance networks shown in Fig.4.5 could be attached to node X, X′ of the circuits in Fig.4.3 so that the gain can be electronically adjusted. Note also that the amplifier bias setting voltages V_{CG} and V_{NO} are supplied from bias circuitries as described in the next section.

4.4 SECOND-ORDER FILTER AND BIASING TECHNIQUE

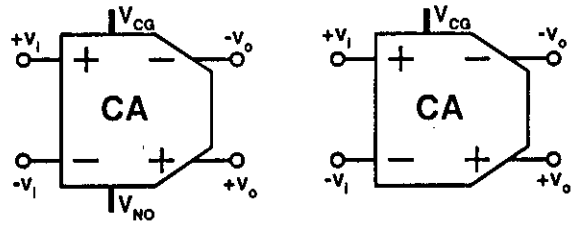
Amplifiers of Fig.4.3 are employed to demonstrate applications in a high-order filter design, here a resonator as shown in Fig.4.6 whose structure is widely known [4.1], [4.2]. The resonator employs a bias network that sets all necessary DC voltages for the whole filter without requiring any additional CMFB amplifiers for each current amplifier.



(a) Class-A output

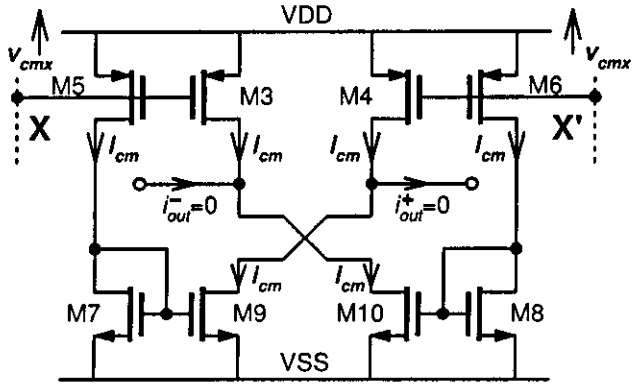


(b) Class-AB output

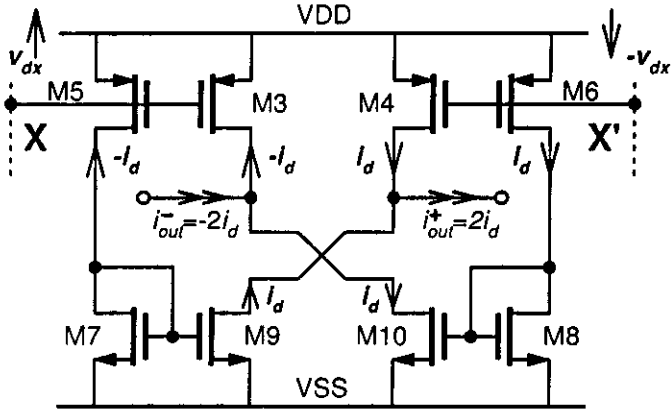


(c) Symbolic representations

Fig.4.3 *Proposed high-gain current amplifiers*



(a) Common-mode: rejection



(b) Differential: addition

Fig.4.4 *Signal handling of the output stage in Fig.4.3b*

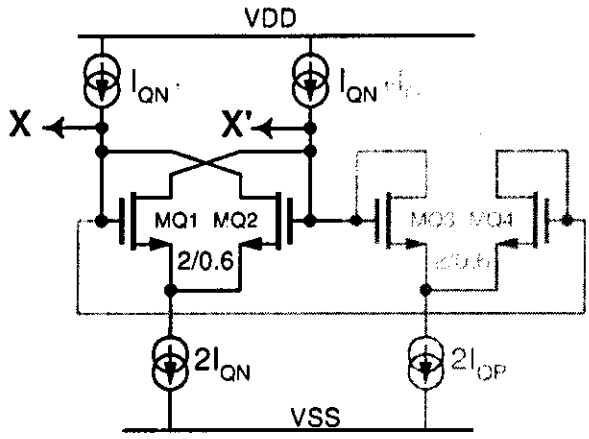


Fig.4.5 *Tuneable negative and positive resistance network*

Such bias set-up network (Fig.4.7) employs a feedback servo loop to set V_{CG} for every current amplifier so that the DC voltage at amplifier's input terminals (sources of MN1 and MN2 in Fig.4.3) is equal to V_{REFi}=V_{SET}. In the filter structure with cascade configuration, it is common to bias amplifiers' input and output terminals at the same DC level to allow optimal signal swing. Therefore, the DC output voltage of each current amplifier should also be set at V_{SET}.

In most cases of MOSFET-C or active-RC filters (cascade configuration) [4.1]-[4.5], there are always interconnections between amplifiers' output and input terminals via resistors (or triode-MOS), and if these resistors carry infinitesimal DC currents, the DC output terminal voltages of the amplifiers will be automatically equal to those of input terminals. The second servo loop in Fig.4.7a with V_{REFo}=V_{SET} is thus needed to make sure that those interconnecting resistors carry no DC currents, where it sets voltage V_{NO} for every single current amplifier in the filter to make sure that M3 and M5 (M4 and M6) carry the same DC bias current. The bias network for the amplifier in Fig.4.3b (Fig.4.7b) does not require a second servo-loop because the output bias current of M3 and M4 is equal to M9 and M10 thanks to a common-mode rejection network as described in the previous section. Therefore the output bias voltage is set via resistor R and it equals V_{REFi}=V_{SET}.

Therefore in a high-order filter design, only *one* of this bias network is needed for the whole filters and it thus helps minimise power consumption and silicon area since no extra CMFB amplifiers are required for DC voltage setting up. The proposed current amplifiers in Fig.4.3 can be readily modified into two-stage OTAs by injecting input voltage signal at gates of M1, M2 with their sources joined together. However, each OTA necessitates high-performance CMFB amplifier at its output to set

up DC bias voltage and maintain filter stability. Such OTAs are thus not suitable for low-power filter design.

4.5 Simulation Results

The resonator of Fig.4.6 was simulated under 1-V supply voltage with V_{SET}=0.5V employing 0.18μm CMOS process. Using low threshold-voltage MOS ($|V_{TN}|$ = 0.25V, $|V_{TP}|$ = 0.25V)

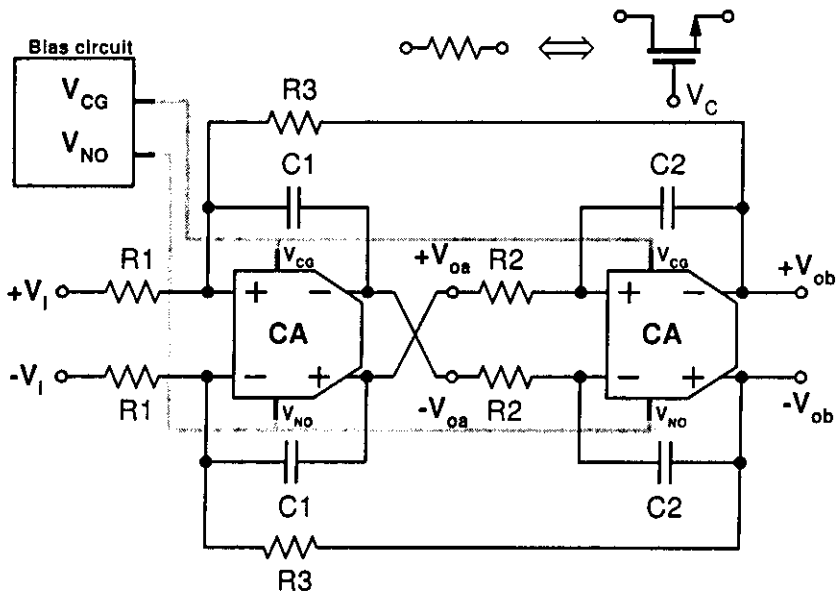
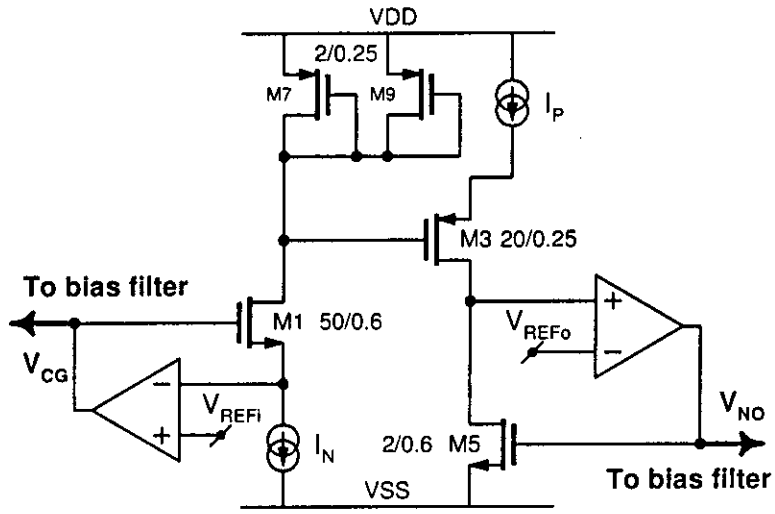
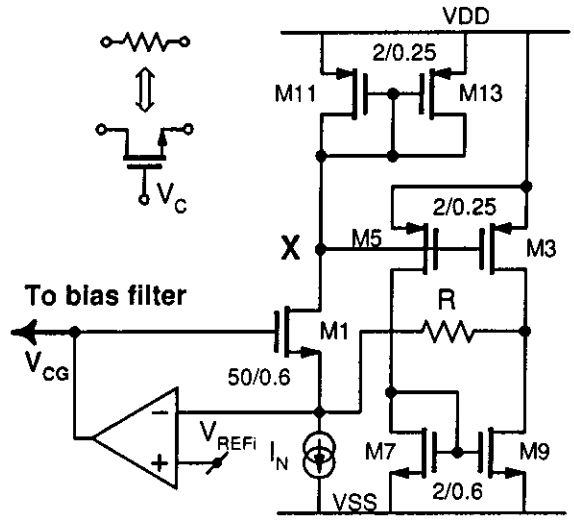


Fig.4.6 *MOSFET-C filter employing the proposed amplifiers.*



(a) For Fig.4.3a

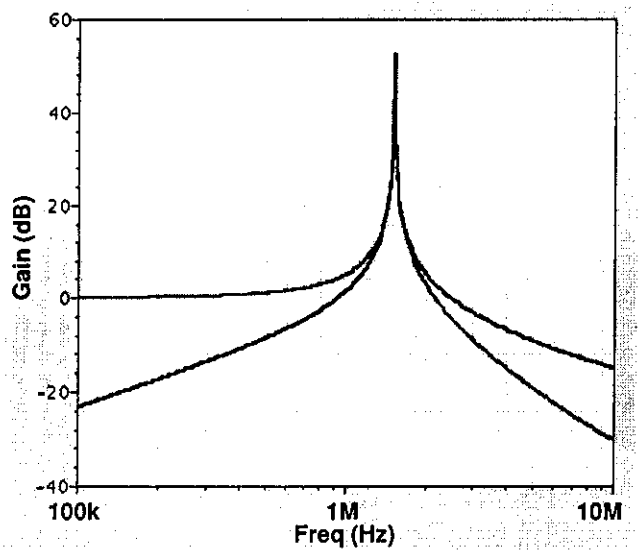


(b) For Fig.4.3b

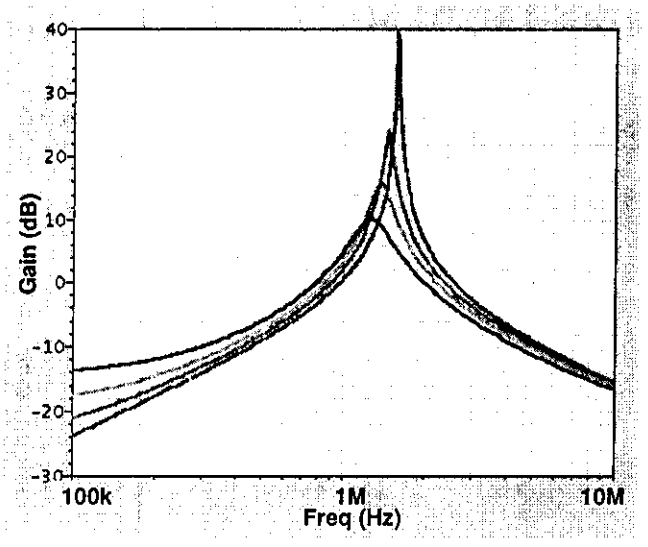
Fig.4.7 *Bias circuitries for MOSFET-C filters in Fig.4.6.*

available in the process, the proposed current amplifier was employed and compared with a conventional balanced folded-cascode OTA ([4.6]). Note that the negative resistance network in Fig.4.5 is also attached at intermediate low-impedance node of such OTA to allow gain enhancement and Q control. Transistor sizes and bias currents between the proposed CAs and the OTA were selected such that these amplifiers consume same bias current and silicon area so that a fair comparison is recognised. However, in the case of the OTA, CMFB amplifiers were employed to set

up DC voltage, i.e., such OTA-RC filter requires more power consumption by design. With $I_N=I_P=2.0\mu A$ (implemented from a simple single-transistor current source), R1=R2=R3=50kΩ (utilising simple triode NMOS transistors), C1=C2=2pF, the filter ac responses are illustrated in Fig.4.8. At Q~10, the total noise of these three filters (lowpass output) were found to be fairly similar and it was equal to ~ $1\times10^{-6}V^2$ (integrated noise from 1Hz to 100MHz). The frequency responses of the filter are depicted in Fig.4.8.



(a) Lowpass and bandpass responses



(b) Q tuning

Fig.4.8 *Second-order filter ac response*

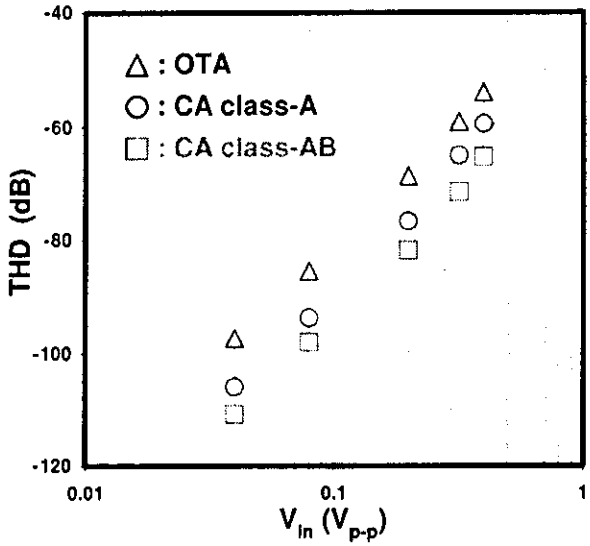
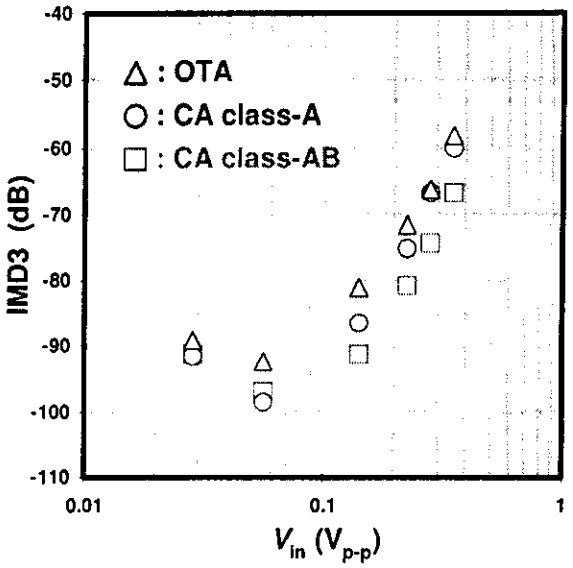
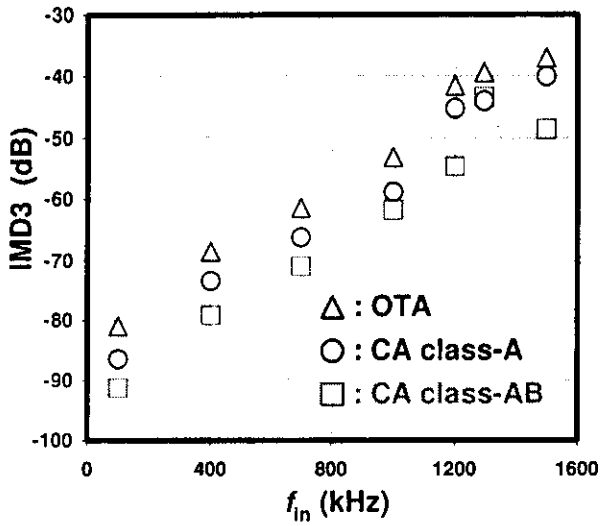


Fig.4.9 *THD comparison at f_{in} = 100kHz*



(a) *f_{in}=100kHz+110kHz*



(b) IMD3 vs frequency

Fig.4.10 *IMD3 comparison*

Distortion performance comparison of the lowpass output (all with Q~10) is shown in Fig.4.9, Fig.4.10 in which both single-tone and two-tone linearity tests are demonstrated, where THD = total harmonic distortion and IMD3 = third-order intermodulation distortion. Fig.4.10b indicates IMD3 comparison with input frequency sweeps from 100kHz to 1500kHz (for roughly constant output magnitude of -26dBVp for each tone). It can be seen that the proposed current amplifiers render superior performance over the conventional OTA. Improvement over 15dB (for THD) and 10dB (for IMD3) has been noticed. Note that due to the fixed current source I_P, the lowpass filters implemented with CA in Fig.4.3a ano the conventional folded-cascode OTA, i.e., class-A output have the same limited input range of $2I_P \cdot R$ = $2\times2.0\mu A\times50k\Omega=\pm0.2V$. Moreover, without a negative resistance network connected to the intermediate low impedance node of the folded-cascode OTA, high-Q cannot be attained and linearity is severely degraded because the transconductance of the OTA is not sufficiently high.

4.6 Conclusion

High-gain current amplifiers have been successfully employed as an alternative active building block to conventional operational amplifiers or operational transconductance amplifier in MOSFET-C and active-RC filters. The second-order filters employing the proposed current amplifiers render better linearity performance over the conventional folded-cascode OTA. Future works include utilisation of the proposed amplifiers in high-order filters similar to those in [4.4], [4.5] for practical applications.

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CHAPTER 5

COMPACT OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS FOR LOW-VOLTAGE MOSFET-C FILTERS

5.1 INTRODUCTION

The MOSFET-C filter design technique has portrayed itself as a simple and effective method for integrating high complexity continuous-time filters on a single CMOS chip with large dynamic range and accurate frequency response [5.1]-[5.4]. It has been demonstrated in [5.1] that, instead of using an operational amplifier (OPAMP), an operational transconductance amplifier (OTA) —— typically consumes less power than OPAMP —— with a sufficiently large transconductance, can be employed as the active building block of the filter. With the push towards low supply voltages in modern fine-line CMOS processes, extensive research efforts have been witnessed on novel low-voltage OTA structures [5.4], [5.5]. This letter introduces a compact two-stage OTA that features a low-voltage class AB output stage with common-mode rejection. The structure and operation of the OTA is described and analysed. This is followed by performance verification via simulation of a 5^{th}-order filter operating under a 0.5-V supply voltage.

5.2 CIRCUIT DESCRIPTION

Fig.1 shows the proposed balanced OTA where its input stage utilises a differential amplifier (N1-N2) with a tail bias resistor R_{ss} and an active load (P1-P2). The use of R_{ss} reduces the voltage headroom requirement compared to that of a tail current source but at the expense of less common-mode rejection. Each side of the balanced output stages consists of two common-source amplifiers (P3-P4 or P5-P6) and a current-mirror load (N3-M4 or N5-N6) with their outputs crossed connected to those of the opposite balanced stage. Such an arrangement offers simultaneous common-mode signal rejection and class AB operation as will be described shortly. The differential cross-coupling transistors ND1-ND4 and NG1-NG4 with the current source I_{BG} are included to emulate large biasing

resistors, similar to that employed in the recent low-voltage OTA [5.4], for setting up the DC voltages V_D and V_G at the drain and gate terminals of N1-N2. The desired quiescent bias levels are controlled by V_{DB} and V_{GB} which are in turn generated by a bias circuitry consisting of two servo loops built around the half-circuit of the OTA. Note that, via a proper sizing, ND1-ND4 can also provide a differential negative resistance for DC gain enhancement [5.4].

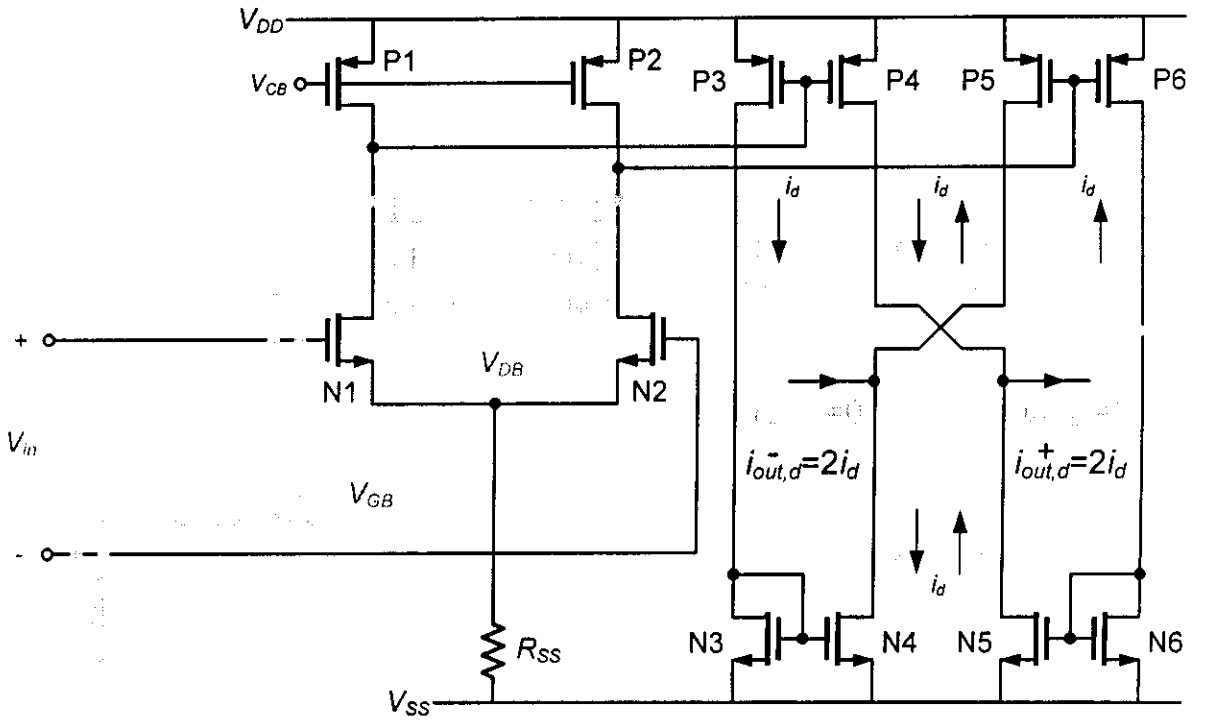

Fig.5.1 *Proposed two-stage OTA.*

The common-mode rejection capability of the output stage can be viewed as a feed-forward operation. This is illustrated by the flow diagram of the common-mode current i_{cm} in Fig.1 (grey arrows) where i_{cm} from P3 (P6) is fed forward by the current mirror N3-N4 (N5-N6) to cancel out i_{cm} from P5 (P4) of the opposite balanced output stage, yielding $i^{+}_{out,cm} = i^{-}_{out,cm} = 0$. On the other hand, from the flow diagram of the differential signal i_d (dark arrows in Fig.1), it can be seen that i_d adds constructively to produce $i^{+}_{out,d} = i^{-}_{out,d} = 2i_d$. Unlike the feed-forward common-mode rejection technique in [5.6], the output stage of Fig.1 also provides a differential current gain factor of two and it thus entails no penalty on the transconductance/bias-current efficiency of the OTA.

To demonstrate the class AB operation, two extreme cases of differential signal excursion are illustrated in Fig.2. On one side of the balanced output stage, the gate voltage, V_{gp}, is above V_{DD} –

$|V_{TP}|$ (or the source-gate voltage $V_{sgp} < |V_{TP}|$) driving all the associated transistors into the cut-off region (as visualised in grey in Fig.2) and hence no output current is supplied. On the other side, V_{gp} is below its quiescent value enabling the transistors on this side to continue supplying the output current to the load Z_L. In effect, the class AB stage operates in a lateral manner where one side of the balanced output can supply the load current while the other side is off. When compared to the conventional push pull complementary MOS stage, this lateral class AB output has potential for a lower voltage operation since the minimum supply voltage requirement is not limited by the gate-source stacking of the conventional push-pull CMOS transistors.

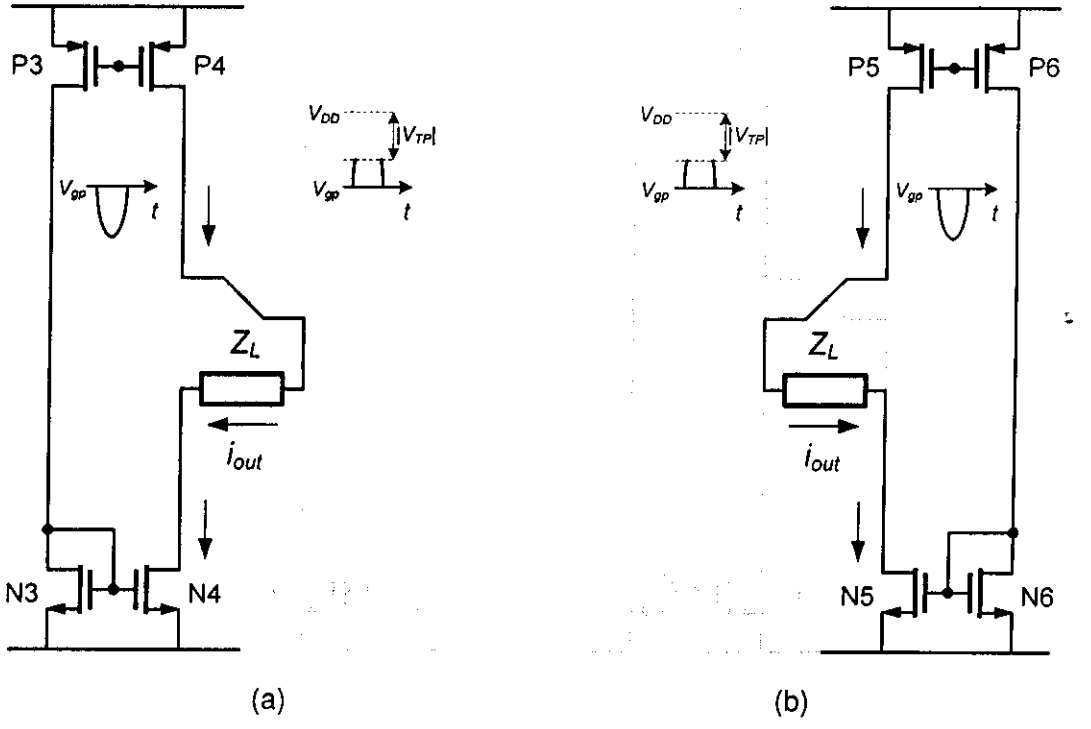

Fig.5.2 *Two extremes of class-AB signal handling.*

Peak voltage swing: When the proposed OTA is employed in an active-RC or MOSFET-C filter, the maximum achievable peak differential output voltage, assuming that the filter employs a single resistive value of R and the OTA's input and output quiescent voltages are set at $V_{DD}/2$, can be derived as

$$V_{out,\max} = V_{DD} + \left(\frac{1}{R \cdot \beta_P} + \frac{1}{R \cdot \beta_N}\right) - \sqrt{\frac{V_{DD}}{R \cdot \beta_P} + \frac{1}{(R \cdot \beta_P)^2}} - \sqrt{\frac{V_{DD}}{R \cdot \beta_N} + \frac{1}{(R \cdot \beta_N)^2}}$$

(5.1)

where $\beta_P = \mu_P C_{ox}(W/L)_P$ is the transconductance parameter of the pMOS amplifier (P3-P6) and $\beta_N = \mu_N C_{ox}(W/L)_N$ is that of the current mirror loads (N3-N6). Based on (1), the dependence of the ratio V_{outmax}/V_{DD} on the product $R \cdot \beta = R \cdot \beta_P = R \cdot \beta_N$ and V_{DD} is shown as a contour plot in Fig.3. The plot suggests that in order for the OTA to achieve the peak voltage swing close to V_{DD}, the product $R \cdot \beta$ should be made large. Since, for a given filter bandwidth ($\propto 1/RC$), the resistance R is normally determined by the required overall filter noise ($\propto 1/C$), β should be selected such that the $R \cdot \beta$ product is sufficiently large. Note, however, that too excessive β ($\propto$ W/L) may result in higher gate capacitances ($\propto$ WL) in the OTA's internal nodes with consequent bandwidth degradation.

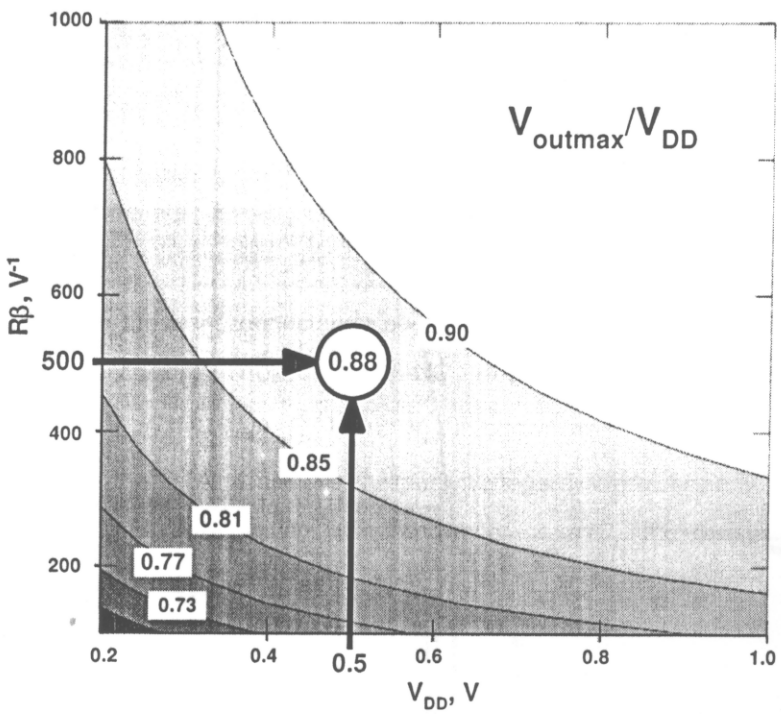

Fig.5.3 *Contour plot of V_{outmax}/V_{DD} as function of V_{DD} and $R \cdot \beta$*

5.3 Simulation Results

By employing the OTA of Fig.1, a 5th-order 100kHz elliptic active-RC filter, with the structure similar to the MOSFET-C filter design in [5.2], was simulated with Spectre using a 2-V 0.18μm CMOS process (V_{TN} = 0.25V, V_{TP} = -0.25V). The transistor dimensions are as follows: N1-N2 =

150/2, N3-N6 = 20/0.3, NG1-NG4 = 20/1, ND1-ND4 = 10/0.6, P1-P2 = 15/3 and P3-P6 = 30/0.25. R_{SS} is at 50kΩ and all the filter resistances R are at 500kΩ. This together with $\beta = \beta_P = \beta_N = 1\text{mA/V}^2$ yields $R \cdot \beta = 500$. At $V_{DD} = 0.5\text{V}$, it is anticipated from (1) (or the plot of Fig.3) that the available peak differential voltage swing is at $0.44V_p$ which is as large as 88% of V_{DD}. Note that all the OTA's inside the filter shared the bias voltages V_{GB}, V_{DB} and V_{CB} that were generated from a single master bias circuitry to set the quiescent voltages V_G and V_D.

Fig.4 shows the frequency responses of the filter under three different supply voltages. For the intended applications at 0.5-V, the filter exhibits the differential peak output of $0.42V_p$ at less than 1% THD for the single-tone test ranging from 10kHz to 90kHz. For the simulated integrated noise at 158 μV_{rms}, this renders the signal-to-noise ratio (SNR) of 65dB. Under the two-tone input test at 50kHz and 55kHz, the spurious-free dynamic range (SFDR) is at 60dB. The filter's SFDR was also simulated at different two-tone inputs (from 10kHz and 15kHz up to 90kHz and 95kHz) for various supply voltages (0.5-V to 1.0-V), and the SFDR was found to be within the range of 56dB to 66dB. The whole filter including the bias circuitry consumes 100μA.

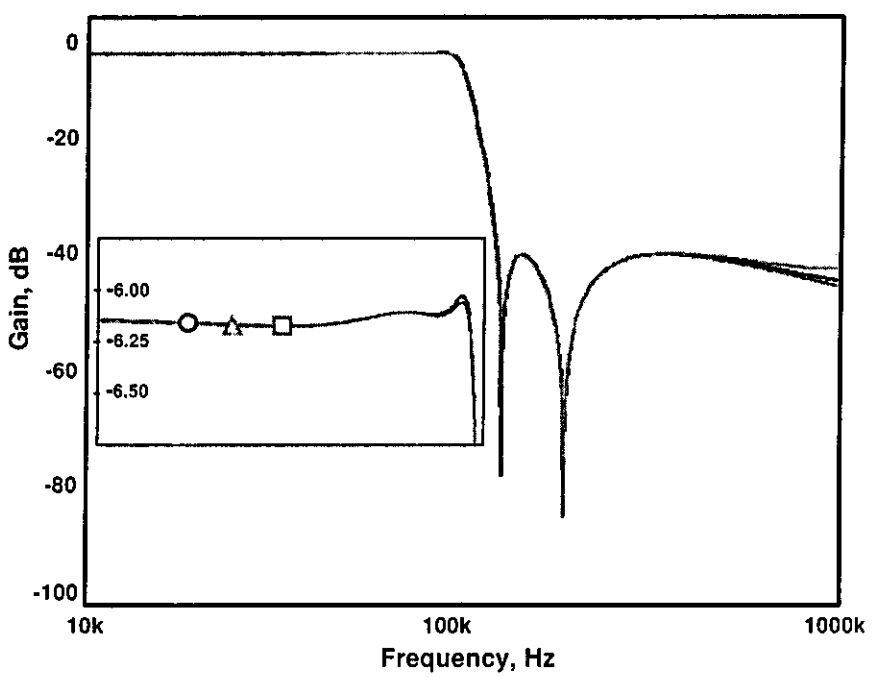

Fig.5.4 *Fifth-order elliptic filter frequency response with V_{DD}: ○ = 1.0V, △ = 0.75V, □ = 0.5V.*

The practicality of the cross-coupled biasing resistors was also confirmed by Monte-Carlo simulation where the standard deviation of both V_G and V_D, due to mismatches of NG1-NG4 and ND1-

ND4, is within 5% of their corresponding quiescent voltages. Also, the filter shows no sign of instability when it is subjected to a rail-to-rail surge of the supply voltage (Fig.5). The simulated SFDR and Figure-of-Merit (FoM), defined by power/(no. of poles × cut-off frequency × SFDR) [5.3] versus supply voltages are depicted in Fig.6.

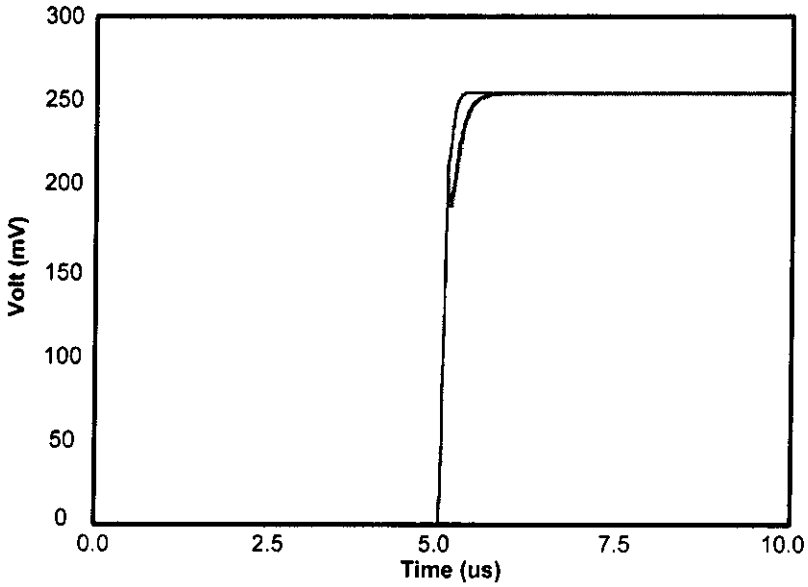

Fig.5.5 *Voltages of OTAs' inputs and outputs responded to a supply step change (from 0V to 0.5V) where the quiescent voltage is designed to be approximately at 250mV.*

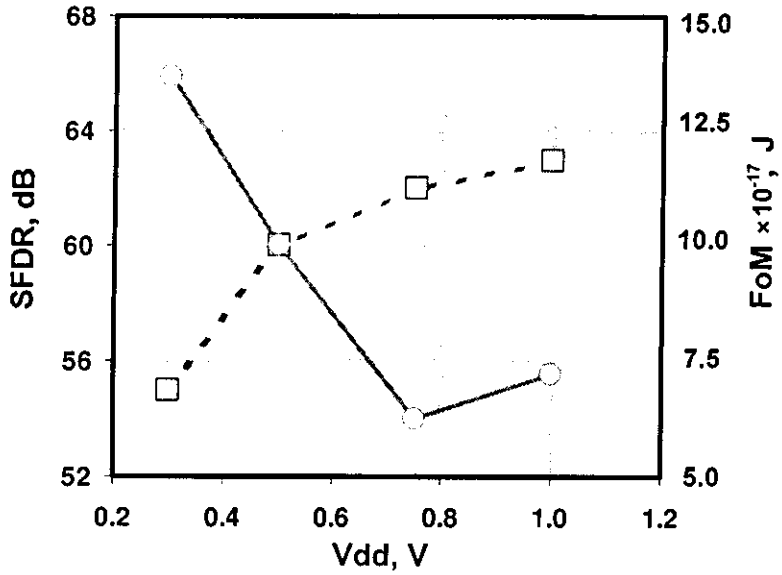

Fig.5.6 *Simulated SFDR, FoM versus V_{DD}:* □ *SFDR,* ○ *FoM*

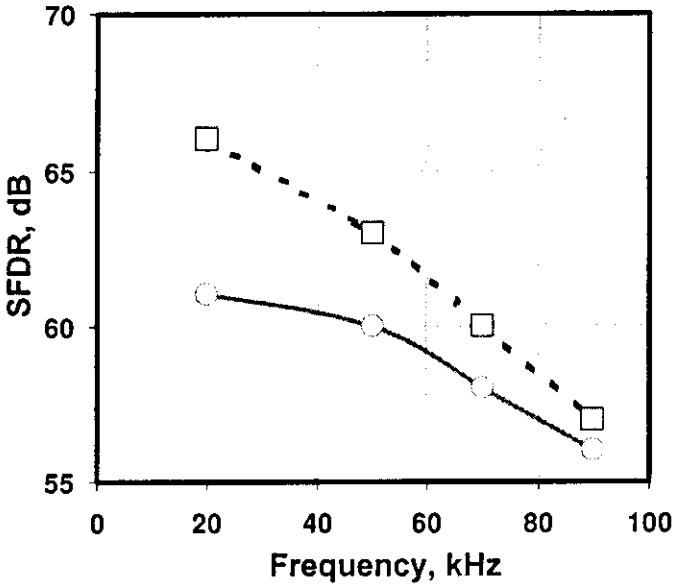

Fig.5.7 *Simulated SFDR at different frequencies V_{DD}: □ 1.0V, ○ 0.5V*

5.4 SUMMARY

A compact OTA suitable for low voltage filter implementations has been developed. The circuit relies primarily on the feed-forward class AB output stage that features low supply operation and common-mode rejection at no cost to transconductance/bias-current efficiency. It is envisaged that the feed-forward output configuration could be applied to current-mode circuits in general or any other circuits with output current variables, such as transconductor (G_m), current conveyor etc. Verified through extensive simulation, it was demonstrated that a low supply voltage filter with a competitive FoM performance at small complexity is entirely viable with the use of the OTA structure.

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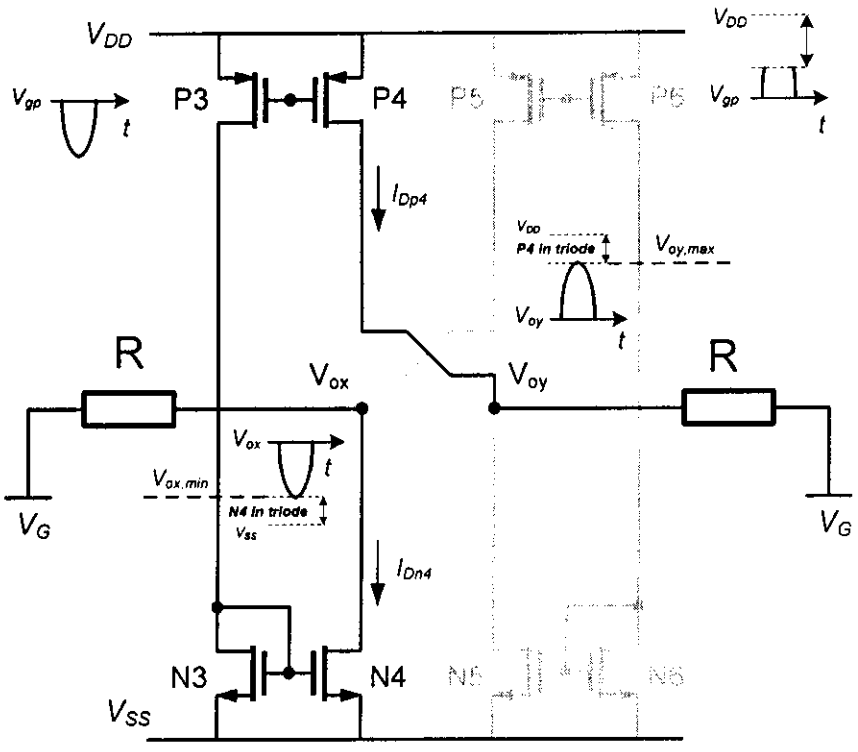
Appendix A5.1 Proof of (5.1)

Derivation of the maximum achievable peak differential output voltage (5.1) is shown as follows.

By assuming that a DC quiescent voltage of the OTA's input and output terminals is at $V_G = V_{DD}/2$. Also when the OTAs are inter-connected inside the filter with negative feedback, **the OTA's input voltage excursion can be assumed to be very small**. Hence the OTA's output stage shown in the figure below can be used for a maximum output voltage swing calculation, where R is a resistor employed for feedback and it can be assumed to be tied to a fixed voltage V_G.



The maximum output swing is calculated when V_{oy} **increases** and V_{ox} **decreases** until P4 and N4 leave saturation region to triode region. This can be estimated by considering when **gate voltage of P3, P4 goes down and gate voltage of P5, P6 goes up in an opposite direction**. Large amount of current is flowing inside P3, P4 (also mirrored to N4) while P5, P6 only carry comparatively very little current, i.e. I_{Dp3}, I_{Dp4} >> I_{Dp5}, I_{Dp6}. Therefore the action of P5-P6, N5-N6 can be ignored.

Consider the first boundary condition when I_{Dp4} is sufficiently large and forces P4 to leave saturation region into triode,

The condition is

$$V_{SDp4} \geq V_{SGp4} - |V_{Tp}| \qquad \text{(A5.1a)}$$

$$V_{DD} - V_{oy} \geq V_{DD} - V_{Gp4} - |V_{Tp}| \qquad \text{(A5.1b)}$$

$$V_{Gp4} + |V_{Tp}| \geq V_{oy} \qquad \text{(A5.1c)}$$

Assuming that I_{Dp4} >> I_{Dn5}, thus the current that flows into *R* on the right hand side mostly comes from I_{Dp4} of P4 (the drain current in triode region), i.e.,

$$\frac{V_{oy}-V_G}{R} \approx I_{Dp4} = \beta_{p4}\left[\left(V_{SGp4}-|V_{Tp}|\right)\left(V_{SDp4}\right)-\frac{\left(V_{SDp4}\right)^2}{2}\right] \quad \text{(A5.2a)}$$

$$\frac{V_{oy}-V_G}{R} = \beta_{p4}\left[\left(V_{DD}-V_{Gp4}-|V_{Tp}|\right)\left(V_{DD}-V_{Dp4}\right)-\frac{\left(V_{DD}-V_{Dp4}\right)^2}{2}\right] \quad \text{(A5.2b)}$$

With $V_{Dp4} = V_{oy}$,

$$\frac{V_{oy}-V_G}{R\beta_{p4}\left(V_{DD}-V_{Dp4}\right)} = \left[\left(-V_{Gp4}-|V_{Tp}|\right)+\frac{\left(V_{DD}+V_{Dp4}\right)}{2}\right] \quad \text{(A5.2c)}$$

$$\left(V_{Gp4}+|V_{Tp}|\right) = \frac{V_G-V_{oy}}{R\beta_{p4}\left(V_{DD}-V_{oy}\right)}+\frac{\left(V_{DD}+V_{oy}\right)}{2} \quad \text{(A5.2d)}$$

Substitute (A5.2d) into (A5.1c) yields,

$$\frac{V_G-V_{oy}}{R\beta_{p4}\left(V_{DD}-V_{oy}\right)}+\frac{\left(V_{DD}+V_{oy}\right)}{2}-V_{oy} \geq 0 \quad \text{(A5.3a)}$$

$$V_{oy}^2-2V_{oy}\left(V_{DD}+\frac{1}{R\beta_{p4}}\right)+V_{DD}^2+\frac{2V_G}{R\beta_{p4}} \geq 0 \quad \text{(A5.3b)}$$

There are two possible solutions to the above equation

$$V_{oya,b} = \left(V_{DD}+\frac{1}{R\beta_{p4}}\right) \pm \sqrt{\left(V_{DD}+\frac{1}{R\beta_{p4}}\right)^2-\left(V_{DD}^2+\frac{2V_G}{R\beta_{p4}}\right)} \quad \text{(A5.3c)}$$

But the only practical solution is the one that renders a voltage swing not exceed V_{DD}, therefore

$$V_{oy,max} = \left(V_{DD}+\frac{1}{R\beta_{p4}}\right) - \sqrt{\left(V_{DD}+\frac{1}{R\beta_{p4}}\right)^2-\left(V_{DD}^2+\frac{2V_G}{R\beta_{p4}}\right)} \quad \text{(A5.3d)}$$

Similarly, consider the other condition just before N4 leaves saturation region into triode when V_{ox} decreases (I_{Dn4} is large),

The boundary condition is

$$V_{DSn4} \geq V_{GSn4} - |V_{Tn}| \quad \text{(A5.4a)}$$

$$V_{ox} \geq V_{Gn4} - |V_{Tn}| \quad \text{(A5.4b)}$$

$$V_{Gn4} - |V_{Tn}| \leq V_{ox} \quad \text{(A5.4c)}$$

By assuming that $I_{Dn4} >> I_{Dp5}$, thus the current that flows into R on the left hand side mostly comes from I_{Dn4} of N4 (the drain current in triode region), we would have

$$\frac{V_G - V_{ox}}{R} \approx I_{Dn4} = \beta_{n4}\left[(V_{Gn4} - |V_{Tn}|)(V_{Dn4}) - \frac{(V_{Dn4})^2}{2}\right] \quad \text{(A5.5a)}$$

$$(V_{Gn4} - |V_{Tn}|) = \frac{V_G - V_{ox}}{R\beta_{n4}V_{ox}} + \frac{V_{ox}}{2} \quad \text{(A5.5b)}$$

Combine (A5.5b) with (A5.4c) gives

$$\frac{V_G - V_{ox}}{R\beta_{n4}V_{ox}} + \frac{V_{ox}}{2} \leq V_{ox} \quad \text{(A5.6a)}$$

$$V_{ox}^2 + 2\frac{V_{ox} - V_G}{R\beta_{n4}} \geq 0 \quad \text{(A5.6b)}$$

And the two solutions of (A5.6b) are

$$V_{oxa,b} = -\frac{1}{R\beta_{n4}} \pm \sqrt{\left(\frac{1}{R\beta_{n4}}\right)^2 + \left(\frac{2V_G}{R\beta_{n4}}\right)} \quad \text{(A5.6c)}$$

But the only practical solution is the one that renders a voltage swing not lower than V_{SS} (= 0V), therefore

$$V_{ox,min} = -\frac{1}{R\beta_{n4}} + \sqrt{\left(\frac{1}{R\beta_{n4}}\right)^2 + \left(\frac{2V_G}{R\beta_{n4}}\right)} \quad \text{(A5.6d)}$$

Hence the maximum output voltage swing before P4 and N4 enter triode region is, $V_{out,max} = V_{oy,max} - V_{ox,min}$ from (A5.3d) and (A5.6d), this renders

$$V_{out,max} = \left(V_{DD} + \frac{1}{R\beta_{p4}}\right) - \sqrt{\left(V_{DD} + \frac{1}{R\beta_{p4}}\right)^2 - \left(V_{DD}^2 + \frac{2V_G}{R\beta_{p4}}\right)} - \left(-\frac{1}{R\beta_{n4}} + \sqrt{\left(\frac{1}{R\beta_{n4}}\right)^2 + \left(\frac{2V_G}{R\beta_{n4}}\right)}\right) \quad \text{(A5.7a)}$$

$$V_{out,max} = V_{DD} + \left(\frac{1}{R\beta_{p4}} + \frac{1}{R\beta_{n4}}\right) - \sqrt{\frac{2V_{DD}}{R\beta_{p4}} + \left(\frac{1}{R\beta_{p4}}\right)^2 - \frac{2V_G}{R\beta_{p4}}} - \sqrt{\left(\frac{1}{R\beta_{n4}}\right)^2 + \left(\frac{2V_G}{R\beta_{n4}}\right)} \quad \text{(A5.7b)}$$

With the OTA's input terminals being biased at half of the supply voltage, i.e. $V_G = V_{DD}/2$, hence

$$V_{out,max} = V_{DD} + \left(\frac{1}{R\beta_{p4}} + \frac{1}{R\beta_{n4}}\right) - \sqrt{\frac{V_{DD}}{R\beta_{p4}} + \left(\frac{1}{R\beta_{p4}}\right)^2} - \sqrt{\left(\frac{V_{DD}}{R\beta_{n4}}\right) + \left(\frac{1}{R\beta_{n4}}\right)^2}$$

Q.E.D.

CHAPTER 6

STRUCTURE OF THE COMPLEX ELLIPTIC GM-C FILTERS SUITABLE FOR FULLY-DIFFERENTIAL IMPLEMENTATION

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Phanumas Khumsat, Prince of Songkla University

6.1 INTRODUCTION

Much research work has been recently focused on the integrated low-IF receivers e.g. [6.1]-[6.7]. The principle of the low-IF receiver is closely related to that of the zero-IF receiver and is based upon the use of quadrature mixing and complex filtering.

Frequency-shifting is a well-known method to transform a real filter into a complex filter. Frequency-shifted complex Gm-C filter can be realized by connecting each pair of the integrating nodes of two identical real filters with a pair of cross-coupled transconductors, as illustrated in Fig. 6.1. The frequency response of the complex filter is the linear frequency-shift version of that of the real filter prototype. However, the method in Fig. 6.1 is possible only for the case of the Gm-C filter without floating capacitor. Therefore, it can be used to complexify only all-pole filters, e.g. Butterworth and Chebyshev filters, not filters with finite zeros such as the elliptic filters.

Method that can be used to transform the single-ended real Gm-C filters with finite zeros into the corresponding single-ended complex Gm-C filters was introduced in [6.8] in which the essential elements are the quadratic imaginary resistors shown in Fig. 6.2(a). Figure 2(b) illustrates the quadratic realization of the single-ended frequency-shifted capacitance obtained by shunting a pair of capacitors with the imaginary resistor in Fig. 6.2(a). However, since the single-ended frequency-shifted capacitance in Fig. 6.2(b) is composed of two fully-differential transconductors, it is not straightforward to convert this quadratic element into the fully-differential structure.

In this paper, the state-space and element substitution methods to transform Gm-C filter, with or without floating capacitors, into complex filters are proposed. Both proposed methods result in the single-ended complex Gm-C filter that employs only single-ended transconductor, a structure that can readily be converted into the fully-differential circuit.

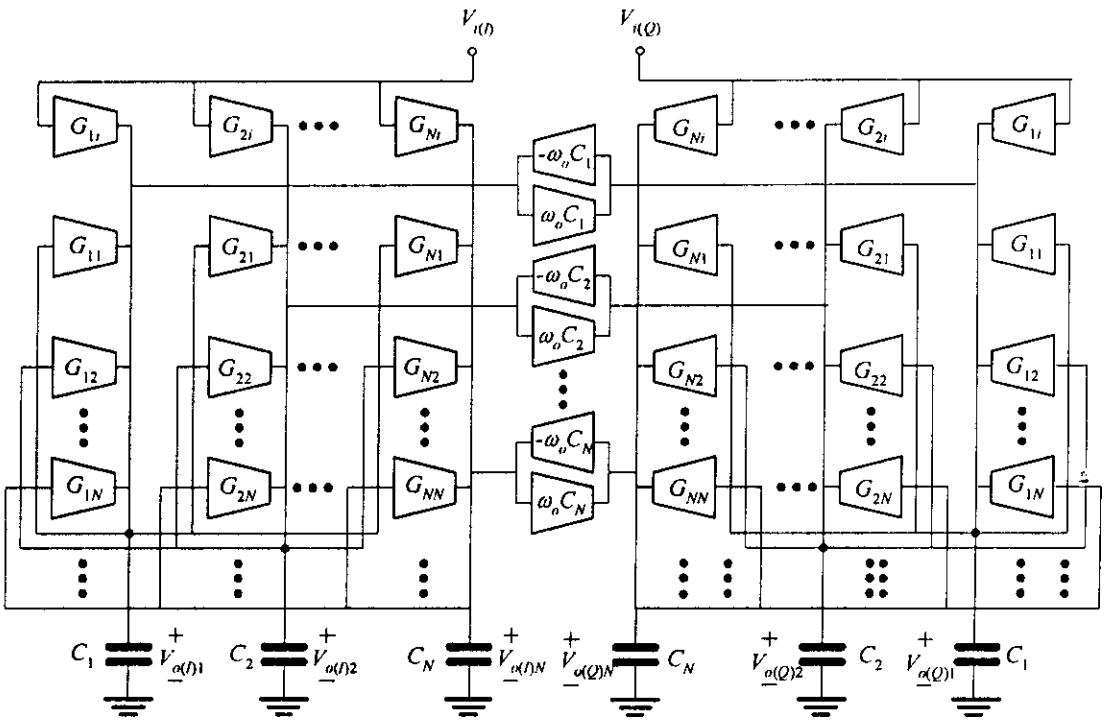
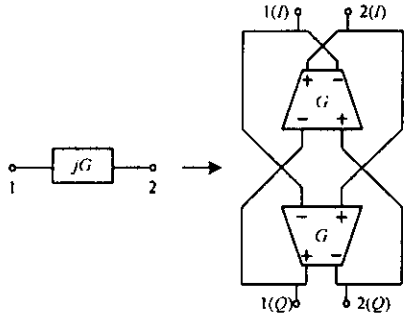
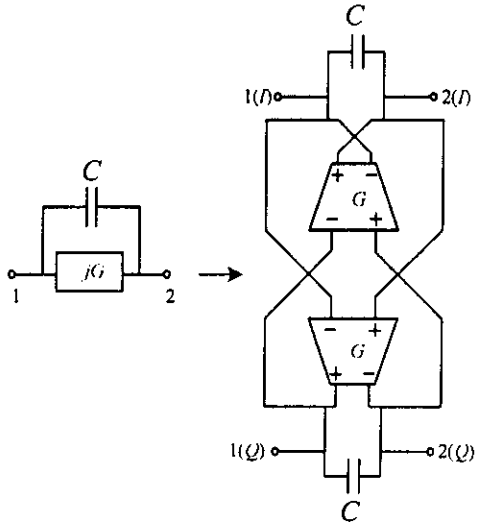


Fig. 6.1 Complex Gm-C filter derived from real Gm-C filter without floating capacitor.



(a)



(b)

Fig. 6.2 Quadratic (I and Q) realization of (a) Single-ended imaginary resistor and (b) Single-ended frequency-shifted capacitance employing a pair of differential transconductors with infinite CMRR [6.8].

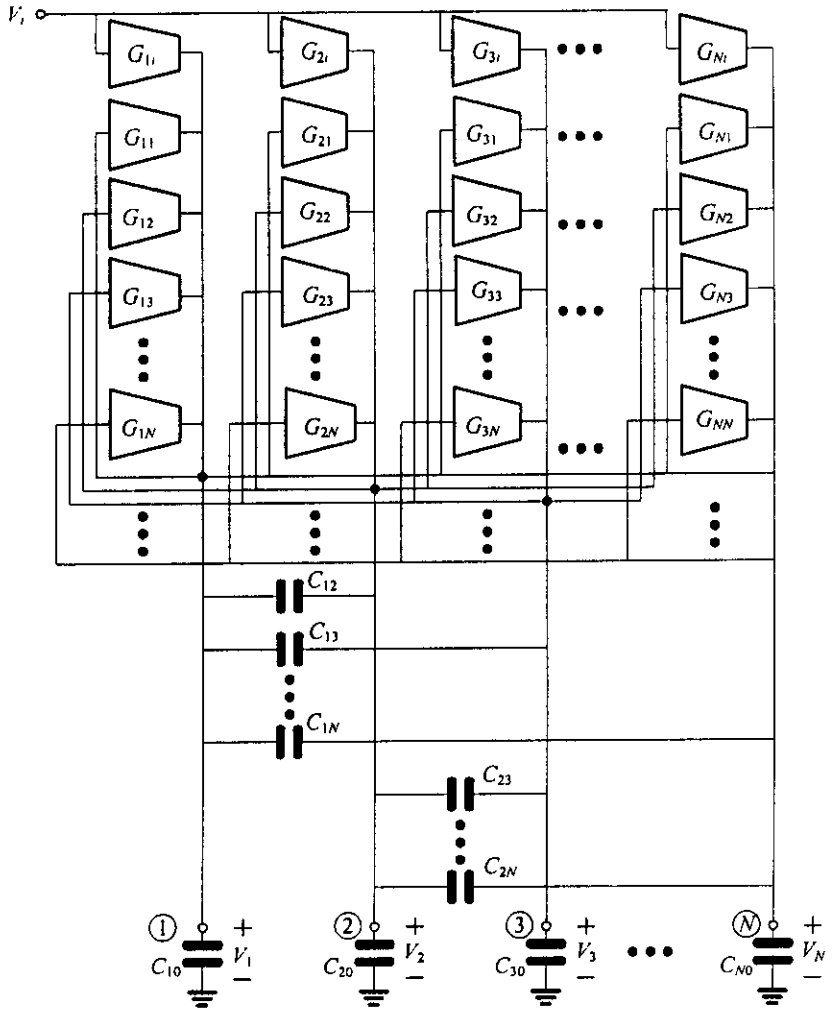


Fig. 6.3 Structure of the Nth-order Gm-C filter.

6.2 COMPLEXIFICATION OF GM-C FILTER USING STATE-SPACE TECHNIQUE

Consider the *Gm-C* filter in Fig. 6.3, which can be mathematically described as [6.12]

$$j\omega\mathbf{CV} = \mathbf{GV} + \mathbf{G}_1 V_i \tag{6.2}$$

where

$$\mathbf{V} = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{bmatrix} \qquad \mathbf{G}_1 = \begin{bmatrix} G_{1i} \\ G_{2i} \\ \vdots \\ G_{Ni} \end{bmatrix}$$

$$\mathbf{G} = \begin{bmatrix} G_{11} & G_{12} & \cdots & G_{1N} \\ G_{21} & G_{22} & \cdots & G_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ G_{N1} & G_{N2} & \cdots & G_{NN} \end{bmatrix}$$

and

$$\mathbf{C} = \begin{bmatrix} \sum_{j=0}^{N} C_{1j} & -C_{12} & \cdots & -C_{1N} \\ -C_{21} & \sum_{j=0}^{N} C_{2j} & \cdots & -C_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ -C_{N1} & -C_{N2} & \cdots & \sum_{j=0}^{N} C_{Nj} \end{bmatrix}$$

in which C_{j0} denotes grounded capacitor at node j, $C_{jk} = C_{kj}$ denotes floating capacitors connected between nodes j and k and $C_{jj} = 0$.

Using (6.2), the frequency responses of the filter can be expressed as

$$\mathbf{V} = \mathbf{H}(\omega)V_i$$

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{bmatrix} = \begin{bmatrix} H_1(\omega) \\ H_2(\omega) \\ \vdots \\ H_N(\omega) \end{bmatrix} V_i \tag{6.3}$$

where

$$\mathbf{H}(\omega) = \left[j\omega\mathbf{C} - \mathbf{G}\right]^{-1}\mathbf{G}_1 \tag{6.4}$$

Without loss of generality, we consider the 3rd-order (N = 3) complex filter in Fig. 6.4. Such a filter comprises a pair of real *Gm-C* filters connected to each other by an array of cross-coupled transconductors.

Referring to Fig. 6.4, for

$$\mathbf{G}_o = \begin{bmatrix} G_{o11} & G_{o12} & \cdots & G_{o1N} \\ G_{o21} & G_{o22} & \cdots & G_{o2N} \\ \vdots & \vdots & \ddots & \vdots \\ G_{oN1} & G_{oN2} & \cdots & G_{oNN} \end{bmatrix},$$

we have

$$\begin{aligned} j\omega\mathbf{C}\mathbf{V}_I &= \mathbf{G}\mathbf{V}_I - \mathbf{G}_o\mathbf{V}_Q + \mathbf{G}_1 V_{i(I)} \\ j\omega\mathbf{C}\mathbf{V}_Q &= \mathbf{G}\mathbf{V}_Q + \mathbf{G}_o\mathbf{V}_I + \mathbf{G}_1 V_{i(Q)} \end{aligned} \tag{6.5}$$

where

$$\mathbf{V}_I = \begin{bmatrix} V_{1(I)} \\ V_{2(I)} \\ \vdots \\ V_{N(I)} \end{bmatrix} \quad \text{and} \quad \mathbf{V}_Q = \begin{bmatrix} V_{1(Q)} \\ V_{2(Q)} \\ \vdots \\ V_{N(Q)} \end{bmatrix}.$$

By defining $V_i = V_{i(I)} + jV_{i(Q)}$ and

$$\mathbf{V} = \begin{bmatrix} V_{1(I)} \\ V_{2(I)} \\ \vdots \\ V_{N(I)} \end{bmatrix} + j \begin{bmatrix} V_{1(Q)} \\ V_{2(Q)} \\ \vdots \\ V_{N(Q)} \end{bmatrix}$$

the above equations can be re-written as

$$j\omega\mathbf{CV} = \mathbf{GV} + j\mathbf{G}_o\mathbf{V} + \mathbf{G}_i V_i \tag{6.6}$$

According to (6.6), for

$$\mathbf{G}_o = \omega_o \mathbf{C} \tag{6.7}$$

it can be shown that

$$j\omega\mathbf{CV} = \mathbf{GV} + j\omega_o\mathbf{CV} + \mathbf{G}_i V_i \tag{6.8}$$

which leads to

$$\mathbf{V} = \mathbf{H}_S(\omega) V_i \tag{6.9}$$

where

$$\mathbf{H}_S(\omega) = \left[j(\omega - \omega_o)\mathbf{C} - \mathbf{G}\right]^{-1}\mathbf{G}_i \tag{6.10}$$

By comparing (6.10) to (6.4), it can be seen that the transfer function $\mathbf{H}_S(\omega)$ can be expressed as

$$\mathbf{H}_S(\omega) = \mathbf{H}(\omega - \omega_o),$$

which is the linear shifted version of $\mathbf{H}(\omega)$.

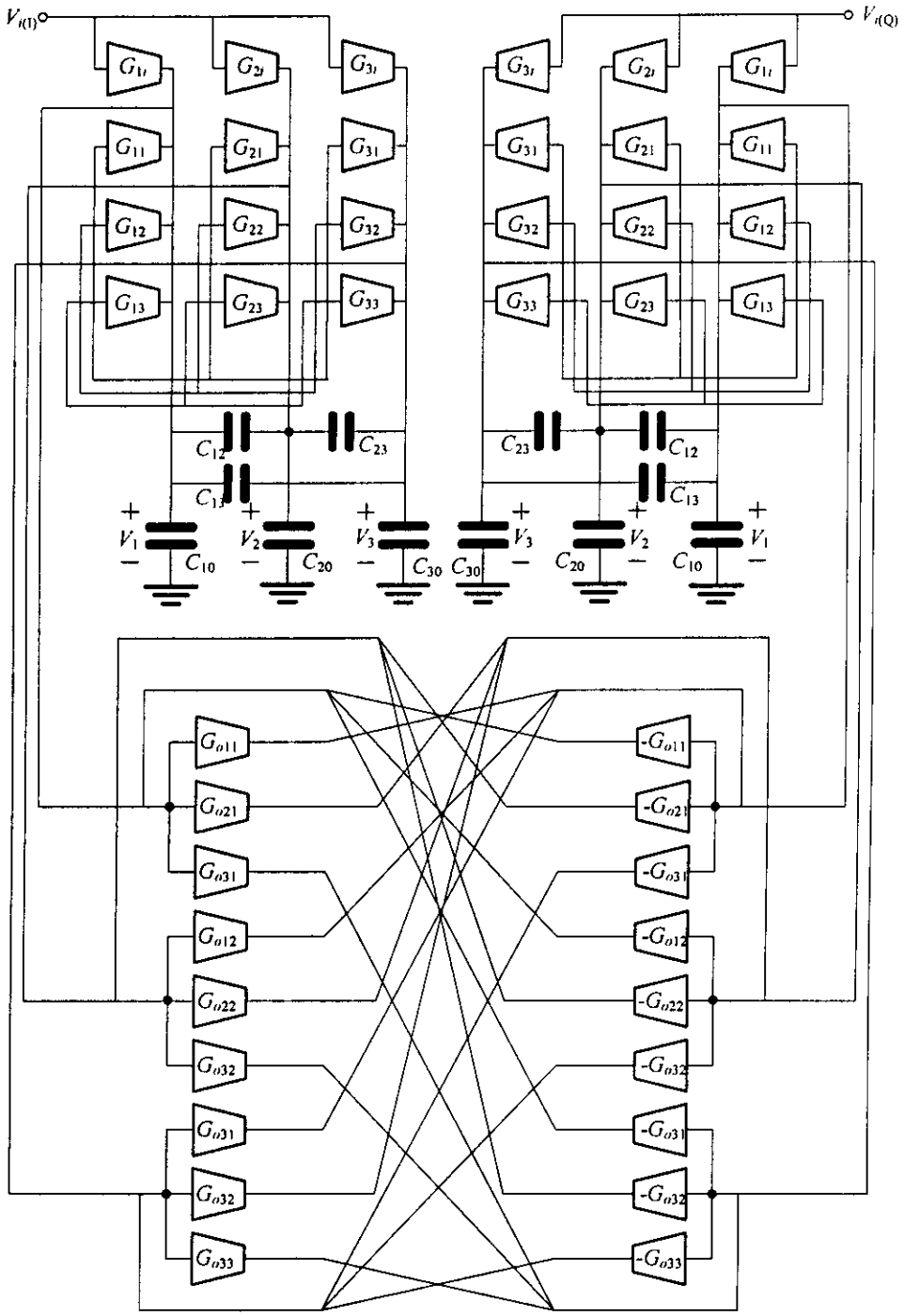


Fig. 6.4 The 3rd-order complex Gm-C filter

6.3 COMPLEXIFICATION OF GM-C FILTER BY ELEMENT SUBSTITUTION TECHNIQUE

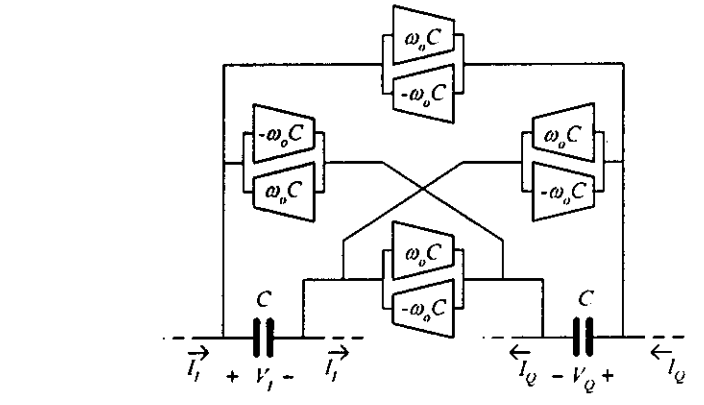
Closely related to the frequency-shifted capacitance in Fig. 6.2(b), Fig. 6.5(a) illustrates the frequency-shifted capacitance composed of eight transconductors and a pair of floating capacitors. According to Fig. 6.5(a), by defining the complex current and voltage variables as

$$I = I_I + jI_Q \quad \text{and} \quad V = V_I + jV_Q ,$$

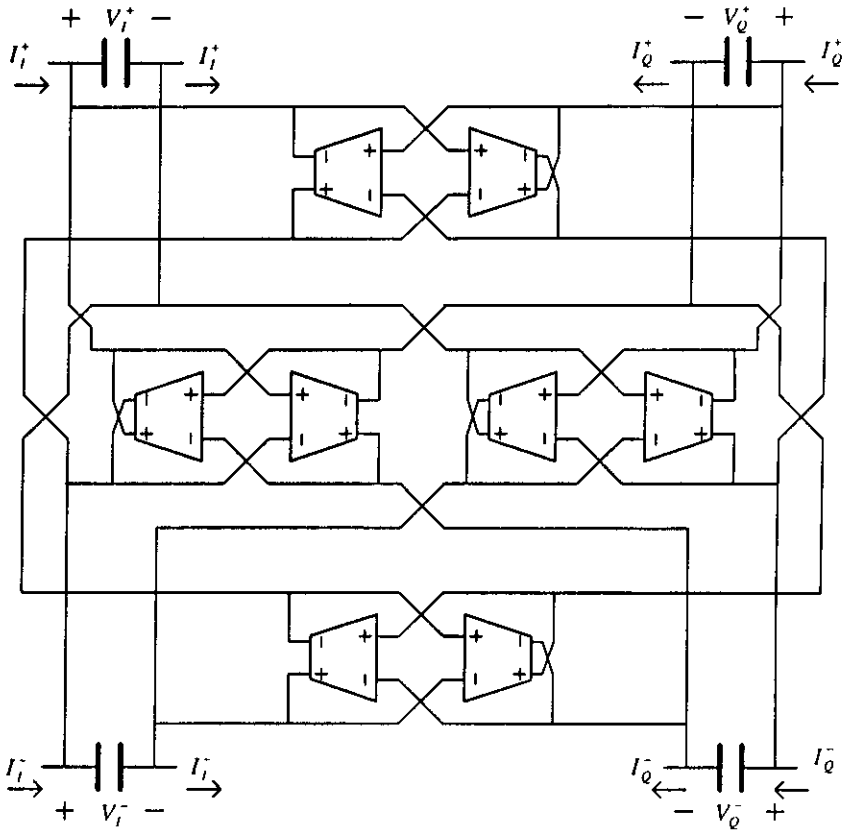
respectively, it can be shown that

$$I = j(\omega - \omega_o)CV \tag{6.11}$$

That is, the effective admittance in Fig. 6.5(a) is $j(\omega - \omega_o)C$, which is the frequency-shifted version of the normal capacitive admittance. As a result, intuitively, linear frequency-shifted complex *Gm-C* filter can be realized by firstly doubling the real *Gm-C* filter prototype into two identical (I and Q) *Gm-C* sections and then connecting each capacitor in the I section to its replica in the Q section with the transconductance network shown in Fig. 6.5(a). The fully-differential realization of the frequency-shifted capacitance in Fig. 6.5(a) is depicted in Fig. 6.5(b). It is worth noting that in the case of grounded capacitors, the network in Fig. 6.5(a) can be reduced to the one shown in Fig. 6.6, which corresponds to the conventional complex filter structure in Fig. 6.1.



(a)



(b)

Fig. 6.5 Quadratic realization of (a) the single-ended floating frequency-shifted capacitance, (b) fully differential realization.

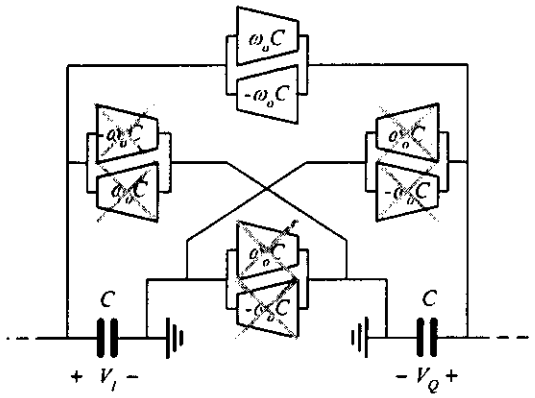


Fig. 6.6 Single-end grounded frequency-shifted capacitance.

6.4 DESIGN EXAMPLE

According to (6.2), the matrices that correspond to the elliptic filter in Fig. 6.7 are

$$\mathbf{G} = \begin{bmatrix} -G & -G & 0 \\ G & 0 & -G \\ 0 & G & -G \end{bmatrix}, \quad \mathbf{G}_I = \begin{bmatrix} G \\ 0 \\ 0 \end{bmatrix}$$

and

$$\mathbf{C} = \begin{bmatrix} 2.178C & 0 & -0.486C \\ 0 & 0.733C & 0 \\ -0.486C & 0 & 2.178C \end{bmatrix}$$

Consequently from (6.7), we have

$$\mathbf{G}_o = \begin{bmatrix} 2.178C\omega_o & 0 & -0.486C\omega_o \\ 0 & 0.733C\omega_o & 0 \\ -0.486C\omega_o & 0 & 2.178C\omega_o \end{bmatrix}$$

According to the above matrices, the complex filter derived from the real *Gm-C* filter of Fig. 6.7 is shown in Fig. 6.8 which is a single-ended structure that can be readily converted into fully differential realization.

Alternatively, by doubling the *Gm-C* filter in Fig. 6.7 into the I and Q sections and connecting each capacitor in I section to its respective duplicated capacitor in the Q section with the transconductance network shown in Fig. 6.5(a) (in case of floating capacitors) and Fig. 6.6 (in case of grounded capacitors), the complex filter in Fig. 6.9 is obtained. It is straightforward to show that by combining all the transconductors that are connected in parallel together, the complex in Fig. 6.9 will become identical to the complex filter in Fig. 6.8.

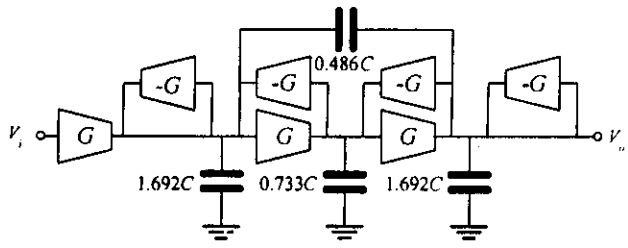


Fig. 6.7 The 3rd-order elliptic *Gm-C* filter ($\omega_p = G/C$) with 1.0 dB passband attenuation ($0 \le \omega \le \omega_p$) and 25 dB stopband attenuation ($\omega > 1.5\omega_p$).

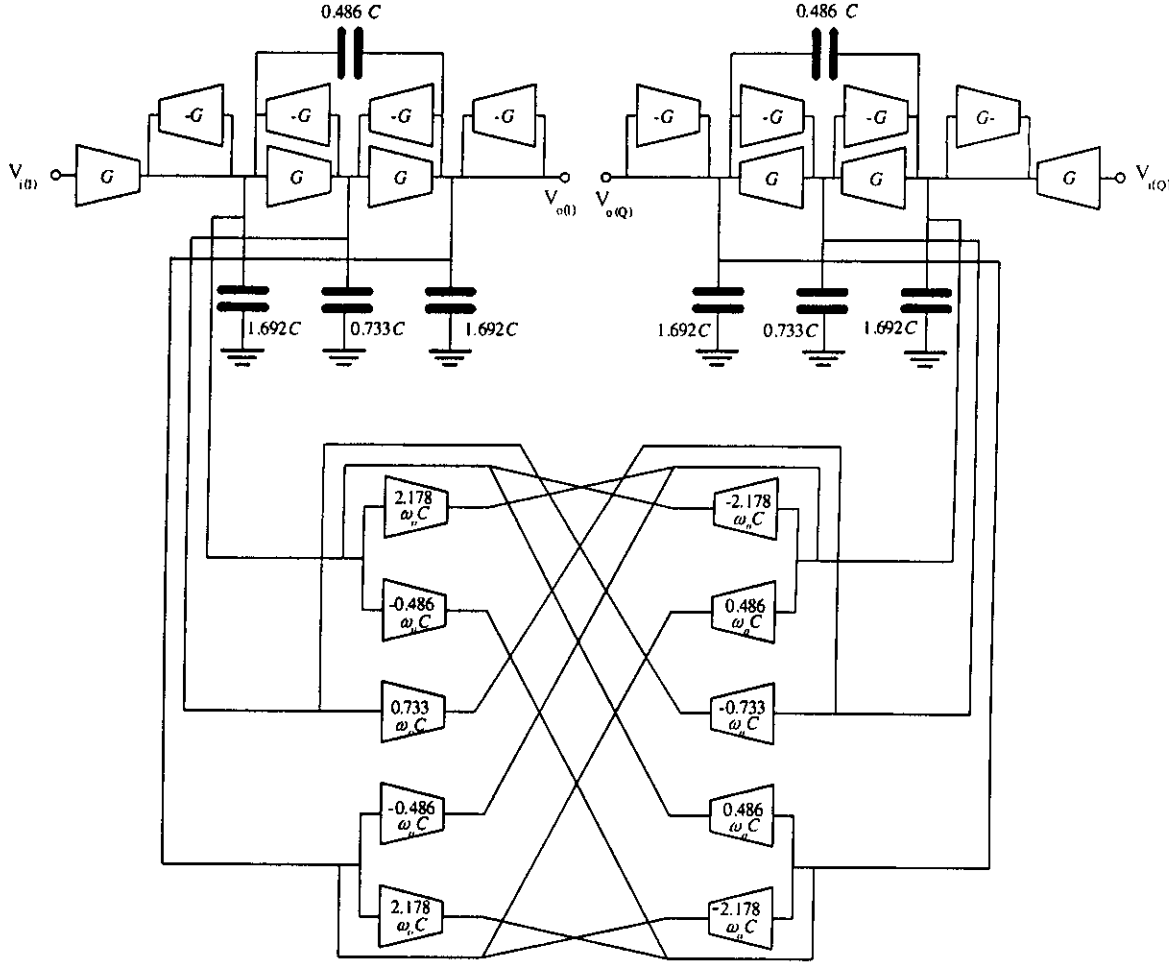


Fig. 6.8 Complex *Gm-C* filter derived from the filter in Fig. 6.6 using state-space technique.

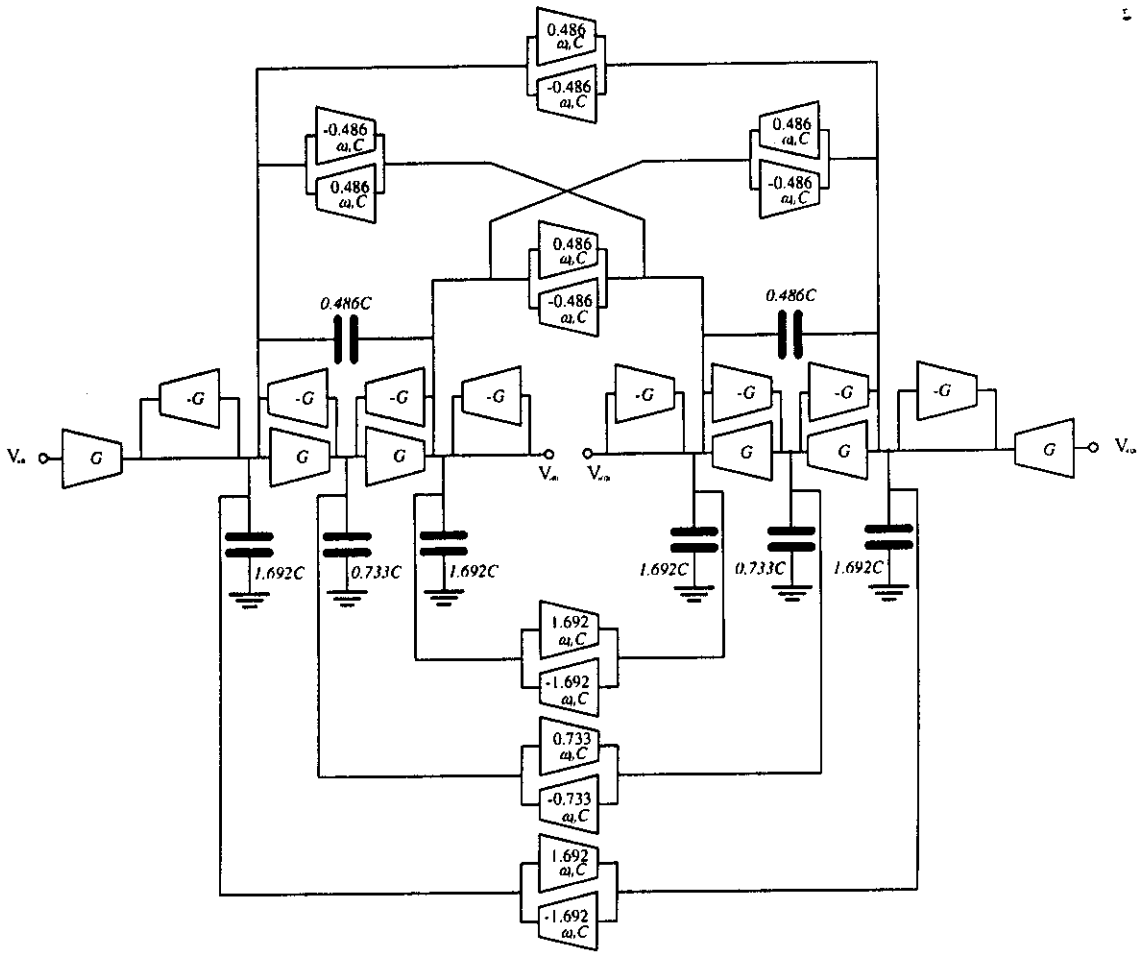


Fig. 6.9 Complex filter obtained by connecting the I and Q sections in accordance with Fig. 6.5 and Fig. 6.6.

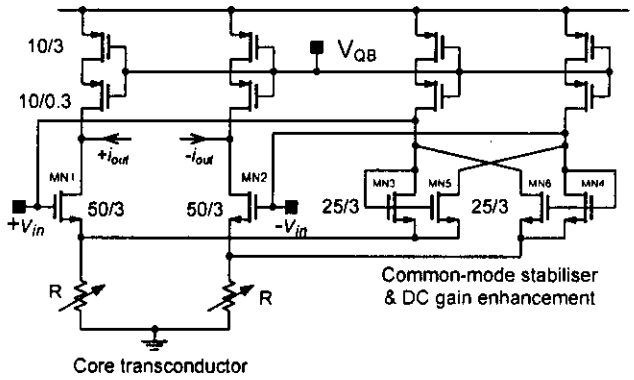
6.5 TRANSISTOR-LEVEL SIMULATION

A practical complex filter has also been designed and simulated based on the proposed Gm-C complexification concept. The differential version of the complex filter in Fig. 6.8 has been implemented such that the resulting filter possesses a bandwidth of 1 MHz and a centre frequency of 500 kHz with G = 20 μA/V, C = 6.37pF, and $\omega_o = 2\pi \times 500$ krad/s.

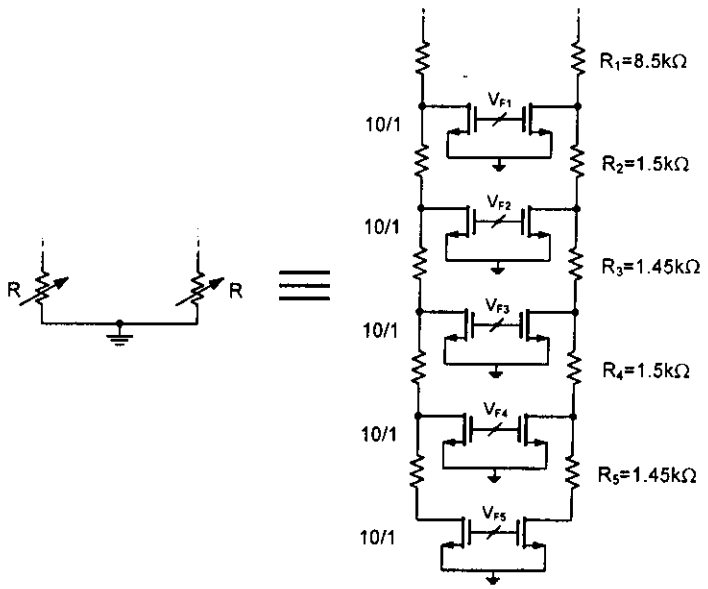
As illustrated in Fig. 6.10, the transconductor employed in the design is the pseudo-differential resistive source-degeneration type [6.9, 6.10] connected with the common-mode stabilizing network [6.11]. The degeneration resistor R can be tuned using a network of linear resistors in series with

triode-MOS resistors (Fig. 6.10b) similar to what has been proposed in [6.10]. Filter tuning can be achieved by adjusting gate voltage of the triode-MOS resistor following the same technique presented in [6.10]. Transistors employed in the common-mode stabilizing network have also been appropriately sized to enhance DC-gain. All the transconductors are biased by simple cascode PMOS current sources whose gate voltage V_{QB} is set by a single network of Fig. 6.11 where transconductor's input and output quiescent voltages are set to be equal to V_{REF}. Two diode-connected MOS (W/L=50μm/3μm) emulate the fact that under a quiescent condition, transistors MN1-MN2 and MN3-MN6 in the common-mode stabilising network resemble a diode-connected NMOS. In this design the quiescent DC voltage is set to be at 1V.

The complex 3rd-order elliptic filter derived from the proposed method has also been compared to the complex filters with the same frequency specifications, namely the 5th-order Chebyshev and the 9th-order Butterworth filters. As the real Butterworth and Cheybyshev filters do not have finite transmission zero, they can be transformed to complex filters by the conventional method (Fig. 6.1). Based on the layout of the unit transconductance cell in Fig. 6.12 and with capacitive trimming to take into account parasitic capacitances, the layouts of the three filters under considerations are depicted in Fig. 6.13. It is clear from Fig. 6.13 that the proposed elliptic filter occupies much smaller area than its Chebyshev and Butterworth filter counterparts. Simulations with parasitic capacitances extracted from the layouts have been conducted using Spectre within Cadence design suite with 3.3-V 0.18-μm CMOS process under 1.8V supply (PMOS and NMOS threshold voltages are ~ 0.45V). Simulations results have been obtained by injecting quadrature signals into the circuits. Simulated AC responses (magnitude and inband group delay) of all the filters are shown Fig. 6.14. Other filter performances including the spurious-free dynamic range (SFDR), 1%-3rd-order-intermodulation-dynamic range (1%-IM3-DR), total capacitance and total transconductors employed, power and current consumption are listed in Table 6.1. It can be observed from Table I that, with the same frequency specifications, the proposed complex elliptic Gm-C filter is more linear, has better noise performance, requires less chip area, and consumes less power than the complex Butterworth and Chebyshev Gm-C filters.



(a)



(b)

Fig. 6.10 (a) Transconductor with common-mode stabilizer and dc gain enhancement (b) Implementation of the source degenerating resistor [6.10].

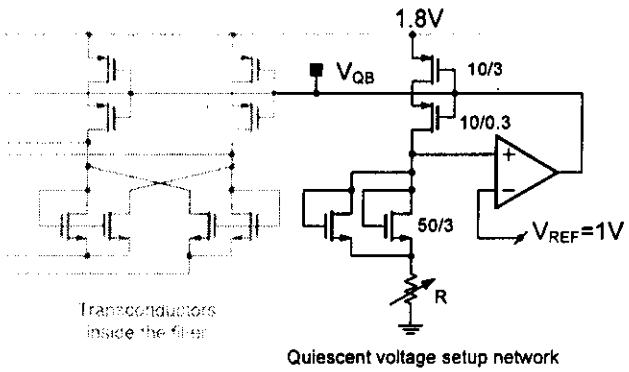


Fig. 6.11 Quiescent-voltage setting-up network for the filter.

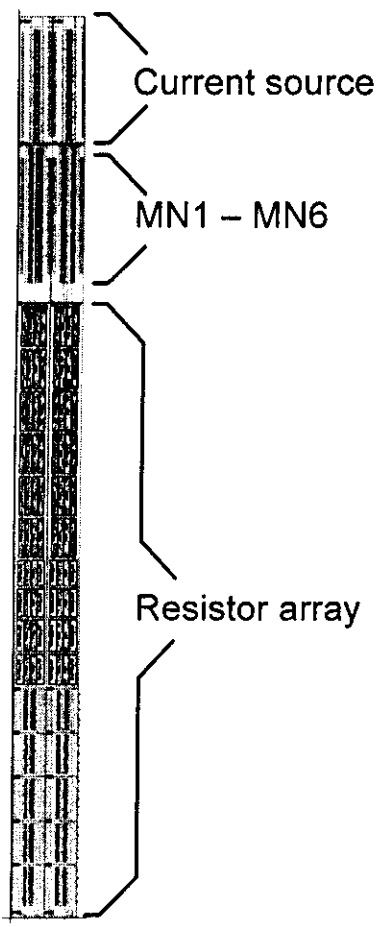


Fig. 6.12 Layout of the transconductor of Fig. 6.10.

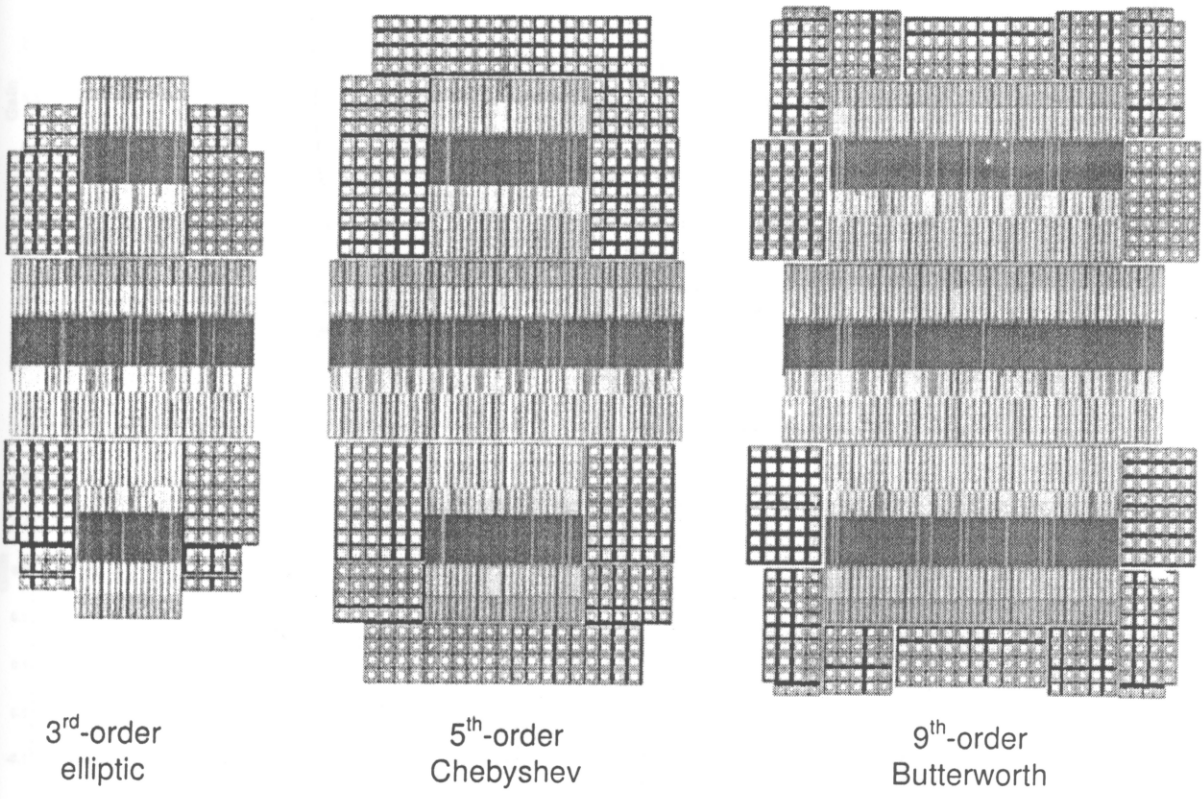
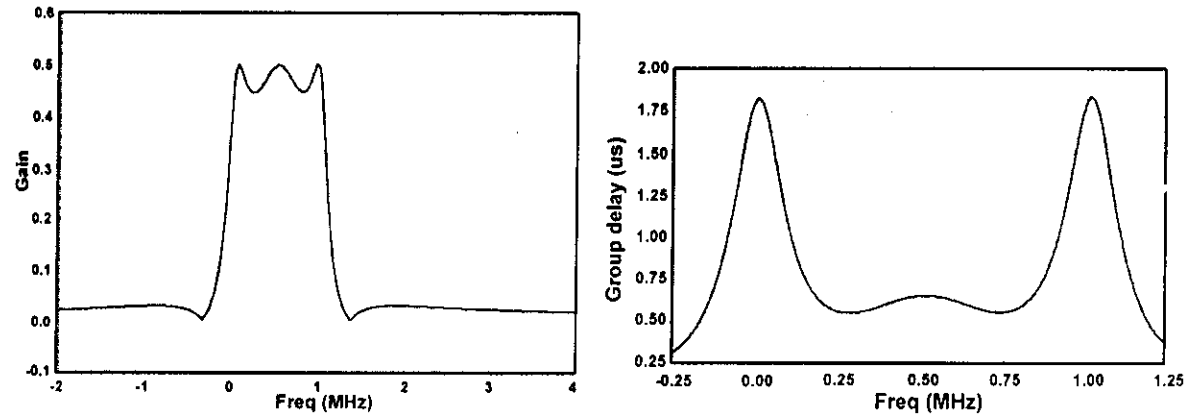
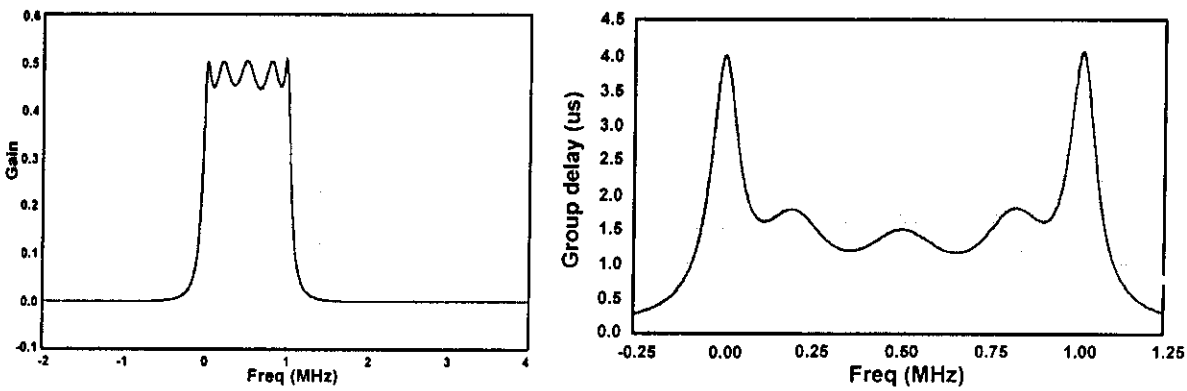


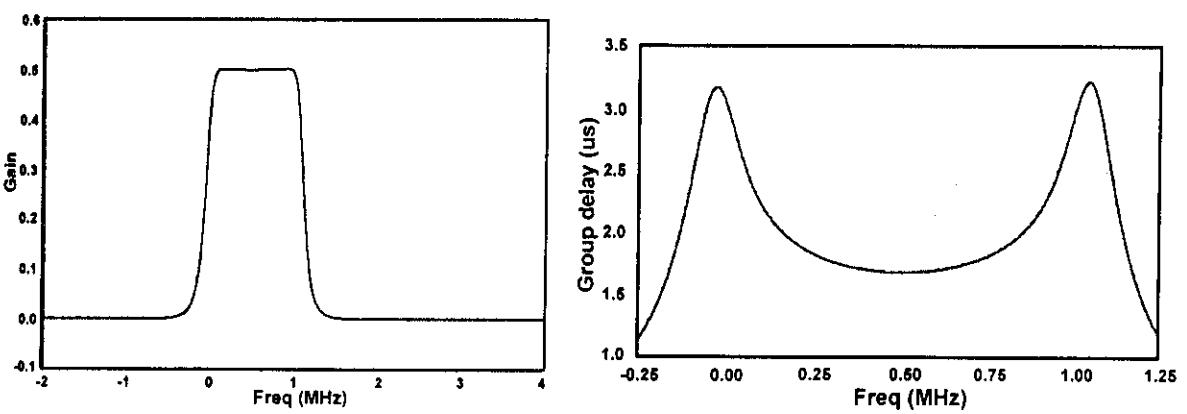
Fig. 6.13 Layouts of the complex Gm-C filters.



(a)



(b)



(c)

Fig. 6.14 Simulated AC simulation results (magnitude and inband group delay) of the complex (a) 3rd-order elliptic filter (b) 5th-order Chebyshev filter (c) 9th-order Butterworth filter.

Table 6.1: Performance comparison of complex filters

Derived from	3^{rd}-order Elliptic	5^{th}-order Chebyshev	9^{th}-order Butterworth
Technology	0.18μm CMOS		
Supply voltage	1.8V		
Output noise integrated from 1Hz to 10MHz	1.96×10^{-7} V^2	2.96×10^{-7} V^2	3.63×10^{-7} V^2
SFDR	47.1dB	44.5dB	43.3dB
1%-IM3-DR	50.1dB	46.8dB	44.7dB
Total integrating capacitance	117.2pF	240.7pF	272.0pF
Total number of unit Gm's	32	48	66
Power consumption (static)	1.54mW	2.14mW	3.01mW
Current consumption (static)	0.86mA	1.19mA	1.67mA
Area	$0.72mm^2$	$1.22mm^2$	$1.59mm^2$

6.4 SUMMARY

We have presented two different methods, basing on state-space and element substitution, to transform the real Gm-C filters with floating capacitors into the corresponding complex Gm-C filters. The resulting complex filter structure is suitable for fully-differential implementation using widely-used fully-differential transconductors. To demonstrate the proposed method, the fully-differential complex Gm-C filter was realized from the 3rd-order elliptic Gm-C filter. It was found that with the same frequency specifications, the elliptic complex filter derived from the proposed method outperforms the Butterworth and Chebyshev complex filters in terms of noise, linearity, area, and power consumption.

6.5 REFERENCES

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CHAPTER 7

CONCLUSION AND FUTURE WORKS

7.1 CONCLUSION

The research work carried in this project has been focused on analog integrated circuit design technique for filtering applications in CMOS and BiCMOS technologies. Achievements in this research can be summarized as follows

- Current-feedback technique has been adopted to improve linearity of the resistive source degenerated transconductor
- MOSFET-C filter employing proposed operational transconductance amplifier (OTA) and operational current amplifier
- Dual-mode feedward technique for enhancing a differential-mode gain and at the same time eliminating common-mode signal.
- Realisation and implementation complex elliptic Gm-C filter which includes floating capacitors

7.2 FUTURE WORKS

Low-voltage techniques investigated from this research can be further developed and integrated into larger systems for low-voltage, low-power applications such as wireless communications and biomedical. To achieve such goal, more critical design issues have to be addressed as listed below

- Low-voltage low-distortion tunable resistor suitable for MOSFET-C filter

- Adaptive phase compensation analysis and design techniques for low-voltage gm-C and active-RC filters without sacrificing power consumption

- Design techniques to overcome common-mode instability for low-voltage active-RC (MOSFET-C) and gm-C filters

- Filter chip layout, fabrication, test and measurement to verify the proposed design techniques.

PUBLICATIONS

Journals

- **P. Khumsat** and A. Worapishet, "Design of 1.8-V CMOS Polyphase Filter for Dual-Mode Bluetooth/ZigBee Transceiver," *The ECTI TRANSACTIONS on ELECTRICAL ENG., ELECTRONICS, and COMMUNICATIONS*, February 2006.
- **P. Khumsat** and A. Worapishet, "Compact Two-Stage Class-AB CMOS OTA for Low-Voltage Filter Applications," *IEICE Transactions on Electronics*, Vol. E90-C, No. 2, February 2007.
- J. Mahattanakul and **P. Khumsat**, "Structure of the complex Elliptic G_m-C filters suitable for fully-differential implementation," *IET Circuits, Devices & Systems*, Vol.1, no. 4, August 2007, pp. 275-282.

Conference proceedings

- **P. Khumsat** and A. Worapishet, "Highly-Linear, Current-Feedback Resistive Source-Degenerated MOS Transconductor," Proceedings of IEEE International Symposium on Circuits and Systems, 2004, Vancouver, Canada.
- **P. Khumsat** and A. Worapishet, "A 1.8-V CMOS Polyphase Filter for Dual-Mode Bluetooth/ZigBee Transceiver," Proceedings of Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology Conference (ECTI-CON), 2005, Pattaya, Thailand.
- **P. Khumsat** and A. Worapishet, "Application of Reverse-Active *npn*s for Compact, Wide-Tuning f_T-Integration-based Filters in SiGe HBT BiCMOS Technology," Proceedings of IEEE International Symposium on Circuits and Systems, 2005, Kobe, Japan.
- **P. Khumsat** and A. Worapishet, "High-Gain Current Amplifiers for Low-Power MOSFET-C Filters," Proceedings of IEEE International Symposium on Circuits and Systems, May 2006, Kos, Greece.

APPENDIX

(Manuscript reprint)

Design of 1.8-V CMOS Polyphase Filter for Dual-Mode Bluetooth/ZigBee Transceiver

Phanumas Khumsat [1] and Apisak Worapishet [2], Non-members

ABSTRACT

A dual-mode Bluetooth/ZigBee low-IF polyphase channel filter has been designed with 0.18 μm digital CMOS technology based upon transconductor-capacitor (GmC) structure. The filter has a fifth-order 0.5dB equiripple Chebyshev bandpass response. It achieves a signal-to-noise ratio of 62dB and input referred third-order intermodulation intercept of 33dBVp (for distant blocker interference). The filter consumes a moderate power of 2.5mW from a 1.8-V single supply in both modes of operation.

Keywords: Transconductor, Gm-C, complex filter, Bluetooth, ZigBee.

1. INTRODUCTION

The low-intermediate frequency (low-IF) polyphase architecture has emerged as the preferred approach for achieving the required sensitivity in fully integrated wireless transceivers [1], [2]. Mainly driven by cost and power consumption, standard CMOS solutions for applications such as Bluetooth (IEEE 802.15.1) and ZigBee (IEEE 802.15.4) have set new challenges for circuit designers at both circuit and system levels. Bluetooth system has widely established itself in various well-known applications including wireless headsets, file sharing and printing, while ZigBee (also known as HomeRF Lite) is used for very simple wireless connectivity. The addition of ZigBee capability to a cell phone could enable the control of devices such as lights, electronic devices and central heating using the mobile handset. A dual-mode transceiver solution is being developed because in the price sensitive market for mobile devices, it is essential that this capability be added for minimal extra cost. Noting that coexistence issue of the two standards on the same frequency band is thoroughly discussed in IEEE Standard 802.15.4.

A polyphase filter or complex filter represents one of the key components in low-IF polyphase receiver. Owing to its asymmetric amplitude response, it has an ability to pass wanted channel signal while efficiently reject neighbouring channel interferers as well as unwanted image.A polyphase filter in this work is based upon transconductor-capacitor structure because of its simplicity, tuneability, linearity and high-frequency performance. The transconductor core circuit follows a linear, wide-tuning, low-noise and compact source degeneration type from [3] where the common-mode feedback and dc gain enhancement has employed a single network according to the topology originally proposed in [4].

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2. REVIEW OF COMPLEX FILTERS

Fig.1 shows the basic principle of the complex filter. Starting with a real low-pass filter, the transformation $s \rightarrow s - \omega_0$ is applied. This shifts the poles up the imaginary axis by ω_0 and transforms the lowpass response into an equivalent bandpass response centred at $\omega = \omega_0$. The transformation preserves both amplitude and phase characteristics and produces the required feature of having no image response at negative frequency. Synthesis of complex filters follows similar procedures to those for real filters except that it makes use of complex integrators. Fig.2 shows transformation from real to complex integrators implemented in the G_mC technique. The transfer characteristic of the complex integrator in Fig.2(b) is described by,

$$H(s) = \frac{i_{out}(s)}{i_{in}(s)} = \frac{G}{(s - j\omega_0)C} \qquad (1)$$

where ω_0 is frequency shift given by $\omega_0 = G_0/C$. This demonstrates that the transformation $s \rightarrow s - \omega_0$ has been performed as required.

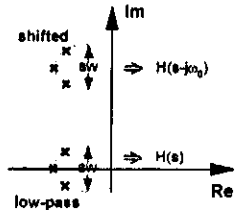

Fig. 1: Complex filter basics

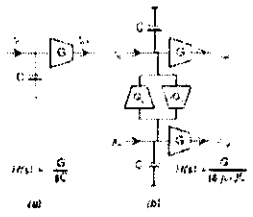

Fig.2: Current-mode Gm-C integrator (a)real (b)complex.

3. TRANSCONDUCTOR CIRCUIT

The variable wide-band resistor source-degeneration transconductor proposed in [3] possesses many advantages including good linearity, low-noise, high frequency capability and low supply voltage. However, such structure inherits a couple of weak points that need special attention. This type of transconductor structure is prone to common-mode instability when employed for filter realisation. It is thus necessary to deploy a common-mode feedback loop comprising common-mode voltage sensing and error amplifiers. Moreover a low dc gain of the transconductor necessitates an additional negative conductance network to provide sufficient dc gain in order to achieve a required filter's frequency response. As depicted in Fig.3, instead of using two separate networks to enhance common-mode stability and dc gain, a single network (MN3-MN6) adopted from the topology presented in [4] is employed. Its main feature is to ensure common-mode stability where the network forms a low impedance load for common signals and a high impedance load from differential signals, effectively resulting in common-mode stability. The technique has been successfully demonstrated with G_mC filters based on an inverter-type transconductor [5]-[9]. The second important feature is to help increase dc gain of the transconductor. And this can be simply achieved by sizing transistors so that a positive feedback current from MN5 MN6 is higher than the negative feedback from MN3 MN4. Two-in-one functionality thus allows additional devices to be kept at minimum; hence this helps save extra silicon area and power consumption. The transconductor in Fig.3 possesses a nominal transconductance value of $20\mu S$ ($V_{P2} = 0.7V$). Note that simple cascode PMOS current sources are employed to supply bias currents to the transconductor. The transconductor also deploys a tuning technique from [3]. Five tuning steps are required in this case to ensure a transconductance continuous sweep of ±50% from the nominal value; each tuning voltage can be varied between 0.6V and 1.8V to adjust degeneration NMOS triode resistance. At any time, only one pair of these degeneration

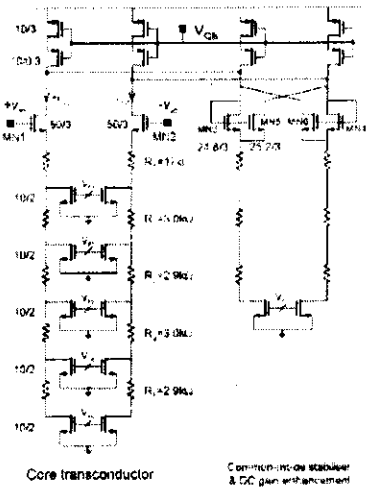

Fig.3: Transconductor with common-mode stabilizer and dc gain enhancement

NMOS's is on and the one-side degeneration resistance R_{de} is (only one V_{Pi} is on)

$$R_{de} = \frac{1}{\mu_n C_{ox}(\frac{W}{L})_1(V_{Pi} - V_{th})} + \sum_{n=1}^{i} R_n \quad (2)$$

μ_n, C_{ox} and V_{th} are conventional parameters for NMOS transistor and the differential transconductance is approximately equal to $1/R_{de}$. To ensure a continuous transconductance sweep, the ladder resistors have to be designed according to (2) so that the adjacent tuning steps have adequate transconductance overlapping at their tuning boundaries when V_{Pi} is switched from one step to another. Because of a limited maximum available tuning voltage of 1.8V, a wide triode resistance variation can be achieved by employing a low threshold voltage NMOS device ($V_{th} = 0.4V$) available in the technology as a tuning triode-MOS resistor. However, it is typical to have large V_{th} for the core transconductor MOS, MN1-MN2. This is because it normally happens that drain and gate voltages swings in opposite directions (sometimes with the same magnitude) from the same quiescent voltage (due to filter's cascade and feedback structure) and having a large V_{th} device will help maintain the transistors in saturation for large signal swing. Note that some of the transistors and resistors within the common-mode stabiliser (drawn in the light shade) can be omitted to save chip area without severely disturbing the circuit operation. It has only

been included in Fig.3 to imitate the core transconductor structure. Compare this transconductor to the class-AB inverter-type MOS transconductor employed for a dual-mode polyphase filter in [7], [8], [9], the proposed transconductor is inherently insensitive to supply voltage variation and it operates in a class-A manner.

4. FILTER DESIGN

A 5th-order 0.5dB equiripple Chebyshev complex filter depicted in Fig.4 is chosen for this work [7]-[9]. The design values for ZigBee and Bluetooth responses are given in Table I. Notice that the design values are half of those used in [7]-[9] in order to minimise power consumption not higher than 2.5mW (this moderate power consumption has also been achieved by the 5th-order polyphase filter in [10]).

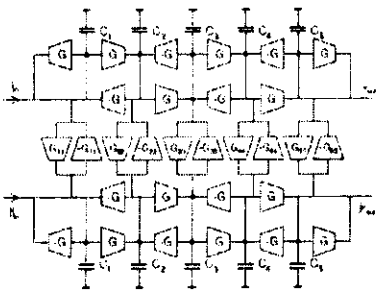

Fig.4: Channel filter architecture.

Table 1: Design values for dual-mode filter

Parameters	Bluetooth	ZigBee
G	$20_{\mu}S$	$20_{\mu}S$
G_{11}	$56.86_{\mu}S$	$56.86_{\mu}S$
G_{22}	$41.99_{\mu}S$	$41.99_{\mu}S$
G_{33}	$84.70_{\mu}S$	$84.70_{\mu}S$
G_{44}	$40.99_{\mu}S$	$40.99_{\mu}S$
G_{55}	$56.86_{\mu}S$	$56.86_{\mu}S$
C_1	$9.05_{p}F$	$4.53_{p}F$
C_2	$6.53_{p}F$	$3.27_{p}F$
C_3	$13.48_{p}F$	$6.74_{p}F$
C_4	$6.53_{p}F$	$3.27_{p}F$
C_5	$9.05_{p}F$	$4.53_{p}F$

A single feedback loop circuit shown in Fig.5 sets quiescent voltage V_{QB} for all transconductors within the filter. The diode-connected MOS ($W/L = 50_{\mu}m/3_{\mu}m$) emulates the fact that under a quiescent condition, transistors MN3, MN5 and MN4, MN6 within the common-mode reject network in Fig.3 resemble a diode-connected NMOS. In this design the quiescent voltage is set to be at 1V. It should be also noted that the op-amp employed in Fig.5 is not required to be high performance, hence it can be easily designed under 1.8-V supply.

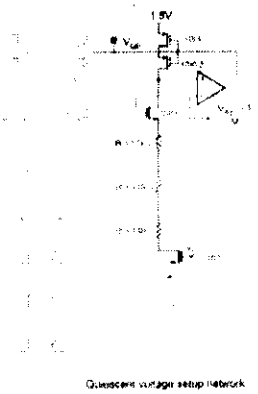

Fig.5: Quiescent voltage setting-up circuitry

5. SIMULATION RESULTS

All the simulations have been carried out using Spectre with Cadence design suite. Simulated frequency response of the complex filter employing 3.3-V 0.18 μm digital CMOS process is shown in Fig.6-Fig.8. It can be seen that the simulated responses are very close to ideal. Note that the actual capacitor values have been trimmed according to the method described in [8] to take parasitic capacitance into account. Fig.6 shows two modes of operation (Bluetooth and ZigBee), obtained by switching the values of capacitor with the common set of transconductors. Fig.7 illustrates frequency tuning at nominal and two extremes by adjusting tuning voltage. This center frequency tuning capability of ¿ 80% is more than enough to encounter process and temperature variations.

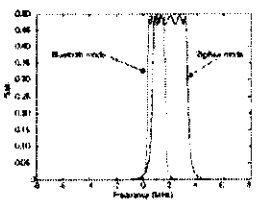

Fig.6: Filter mode switching

The filter common-mode rejection ability has been investigated by measuring common-mode signal fre-

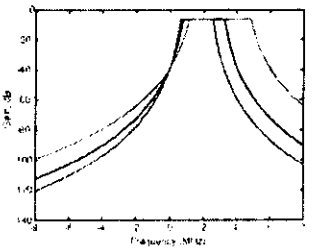

Fig.7: Frequency tuning in ZigBee mode

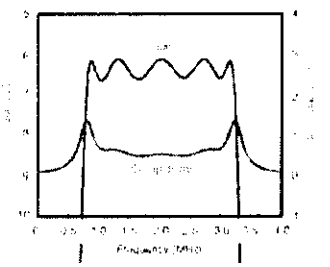

Fig.8: ZigBee's passband response

quency response and compare with differential signal as show in Fig.9. It can be seen that although the structure of Fig.3 does not reject common-mode signal locally, but globally the filter does have ability to suppress common-mode signals. The filter has also been subjected to a transient common-mode step response stability test [3], and the results guarantee its unconditional stability as illustrated in Fig.10.

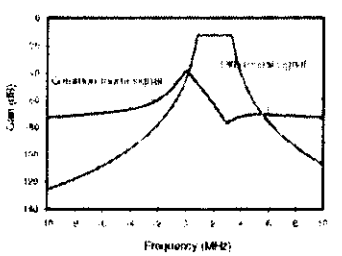

Fig.9: Filter's frequency response: differential vs common-mode (single-end output)

The ZigBee output differential noise is shown in Fig.11 where the total output noise integrated over the 100MHz bandwidth renders output noise power

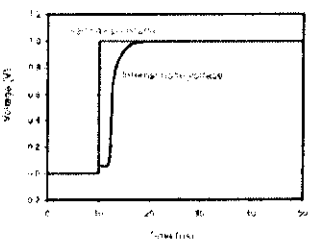

Fig.10: Stability test with step response

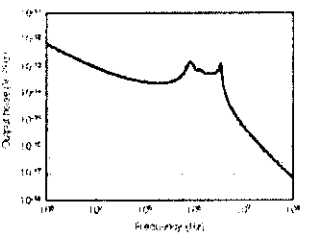

Fig.11: Noise response (ZigBee mode)

voltage of $2.5 \times 10^{-7} V^2$. The ZigBee signal compression characteristic of ZigBee-mode filter is shown in Fig.12 and it demonstrates a linear gain up to an input amplitude of 1Vp (0dBVp) differential and an input referred 1-dB compression point of 1.59Vp (or 4.03dBVp) differential (with corresponding output voltage of 0.68Vp). The signal-to-noise ratio is thus found to be 62.3dB. The in-band spurious free dynamic range (SFDR), where the inter-modulation product has the same power as the filter noise, is found to be 51.3dB and 53.4dB for ZigBee and Blue-

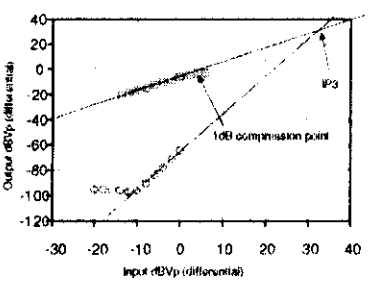

Fig.12: Third-order intermodulation)

tooth modes respectively. Out-of-band intermodulation of the distant blockers was also simulated as also shown in Fig.12 for ZigBee case (inputtones at 6MHz and 10MHz for ZigBee and 3MHz and 5MHz for Bluetooth). It shows the ZigBee third-order intermodulation characteristic indicating an input referred third-order intercept point (IIP3) of 33dBVp differential with corresponding out-of-band SFDR of 59.6dB. The whole filter draws a total current of 1.38mA from a single 1.8-V supply. The overall performance for both modes is summarised in Table 2.

Table 2: Summarised filer performance

Filter Response	Chebyshev	
Filter Order	6+5	
Filter ripple	0.5dB	
Supply voltage	1.8V	
Process	3.3V, 0.18$_\mu$ mCMOS	
Supply current	1.38mA	
Mode	Bluetooth	ZigBee
Centre Frequency	1MHz	2MHz
Bandwidth	1.2MHz	2.4MHz
Bandwidth	1.2MHz	2.4MHz
Gain	-6.18dB	-6.18dB
Output noise	$1.4 \times 10^{-7}V^2$	$1.4 \times 10^{-7}V^2$
Input 1dB Comp.	1.59Vp	1.59Vp
Signal/Noise (SNR)	64.9dB	62.8dB
IIP3 (distant blocker)	36.4dBVp	33dBVp
SFDR		
(a)Distant blocker	62.1dB	59.6db
(b) In-band	53.4dB	51.3dB

6. CONCLUSION

A 1.8V CMOS dual-mode fifth-order polyphase Gm-C filter for Bluetooth/ZigBee transceiver has been designed. The complex bandpass filter is based on Gm-C filter structure with appropriate crossing transconductors to shift lowpass response to the required IF frequencies. It deploys a simple source degeneration transconductor integrated with a network, which could simultaneously provide common-mode stability and dc gain enhancement.

ACKNOWLEDGEMENT

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LETTER

Compact Two-Stage Class-AB CMOS OTA for Low-Voltage Filtering Applications

Phanumas KHUMSAT[†a)], *Nonmember and* Apisak WORAPISHET[††], *Member*

SUMMARY A compact OTA suitable for low-voltage active-RC and MOSFET-C filters is presented. The input stage of the OTA utilises the resistive tail-based differential amplifier and the output stage relies upon the feed-forward class AB technique with common-mode rejection capability that incurs no penalty on transconductance/bias-current efficiency. Analysis on the achievable peak voltage swing of the OTA when employed in filters is given. Simulation results of a 0.5-V 100-kHz elliptic 5th-order filter based on the OTA's in a 2-V 0.18 μm CMOS process indicate the differential peak voltage as large as 0.42 V_{pp} (84% of the supply voltage) at 1% THD with the SFDR of 60 dB and the total power consumption of 50 μW.

key words: operational transconductance amplifier, OTA, active-RC filters, MOSFET-C filters

1. Introduction

The MOSFET-C filter design technique has portrayed itself as a simple and effective method for integrating high complexity continuous-time filters on a single CMOS chip with large dynamic range and accurate frequency response [1]–[4]. It has been demonstrated in [1] that, instead of using an operational amplifier (OPAMP), an operational transconductance amplifier (OTA) — typically consumes less power than OPAMP — with a sufficiently large transconductance, can be employed as the active building block of the filter. With the push towards low supply voltages in modern time-line CMOS processes, extensive research efforts have been witnessed on novel low-voltage OTA structures [4], [5]. This letter introduces a compact two-stage OTA that features a low-voltage class AB output stage with common-mode rejection. The structure and operation of the OTA is described and analysed. This is followed by performance verification via simulation of a 5th-order filter operating under a 0.5-V supply voltage.

2. Operational Transconductance Amplifier

Figure 1 shows the proposed balanced OTA where its input stage utilises a differential amplifier (N1-N2) with a tail bias resistor R_{SS} and an active load (P1-P2). The use of R_{SS} reduces the voltage headroom requirement compared to that of a tail current source but at the expense of less common-mode rejection. Also, to promote very low supply voltage requirement, saturated *moderate to weak inversion* operation similar to the pseudo-differential input pair in [4] should be adopted for N1-N2 where their quiescent gate-source voltage is set at below their threshold voltage. For the balanced output stage, each side of the circuit consists of two common-source amplifiers (P3-P4 or P5-P6) and a current-mirror load (N3-M4 or N5-N6) with their outputs crossed connected to those of the opposite balanced stage. Such an arrangement offers simultaneous common-mode signal rejection and class AB operation as will be described shortly. It should be noted that the output stage transistors can also operate in moderate inversion at *quiescent* conditions. But when a large signal is applied, their operations will be moved to strong inversion for larger current handling in a class-AB fashion. This is in contrast to the input amplifier N1-N2 whose operation always stays in moderate inversion due to the virtual ground created at their inputs when the OTA is employed inside filter structure due to high gain negative feedback loops.

The differential cross-coupling transistors No1-No4 and Ng1-Ng4 with the current source I_{BC} are included to emulate large biasing resistors, similar to that employed in the recent low-voltage OTA [4], for setting up the DC voltages V_D and V_G at the drain and gate terminals of N1-N2. The desired quiescent bias levels are controlled by V_{DB} and V_{GB} which are in turn generated by a bias circuitry consisting of two servo loops built around the half-circuit of the OTA. Note that, via a proper sizing, No1-No4 can also provide a differential negative resistance for DC gain enhancement [4]. In typical MOSFET-C or active-RC filter structures (ladder-based, cascaded etc.), there are always interconnections between the *output* and *input* terminals of the same or different OTA stages through triode-biased MOSFET or linear resistors R. Following this, since the input DC voltage of the proposed OTA of Fig. 1 is set at a well-defined voltage V_G, the output DC voltage for each of the OTA's is automatically set at the same V_G, if the filter resistors R carry infinitesimal DC currents as of typical cases. To allow optimal signal voltage swing, the OTA's input and output terminals are normally set at $V_G = V_{DD}/2$.

The common-mode rejection capability of the output stage can be viewed as a feed-forward operation. This is illustrated by the flow diagram of the common-mode current i_{cm} in Fig. 1 (grey arrows) where i_{cm} from P3 (P6) is fed forward by the current mirror N3-N4 (N5-N6) to can-

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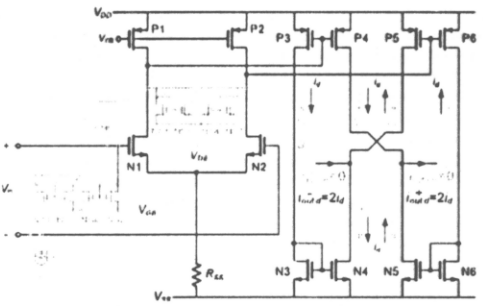

Fig. 1 Proposed two-stage OTA.

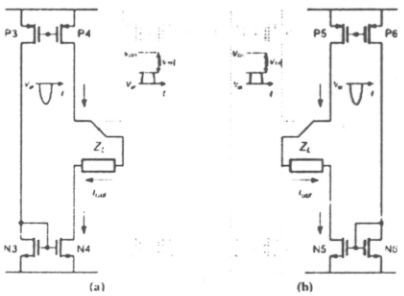

Fig. 2 Two extremes of class-AB signal handling.

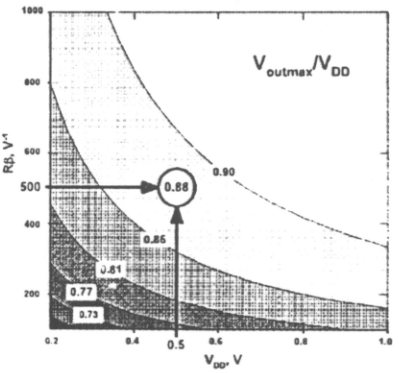

Fig. 3 Contour plot of $V_{out\,max}/V_{DD}$ as function of V_{DD} and $R \cdot \beta$.

cel out i_{cm} from P5 (P4) of the opposite balanced output stage, yielding $i_{out,cm}^+ = i_{out,cm}^- = 0$. On the other hand, from the flow diagram of the differential signal i_d (dark arrows in Fig. 1), it can be seen that i_d adds constructively to produce $i_{out,d}^+ = i_{out,d}^- = 2i_d$. Unlike the feed-forward common-mode rejection technique in [6], the output stage of Fig. 1 also provides a differential current gain factor of two and it thus entails no penalty on the transconductance/bias-current efficiency of the OTA.

To demonstrate the class AB operation, two extreme cases of differential signal excursion are illustrated in Fig. 2. On one side of the balanced output stage, the gate voltage, V_{gp}, is above $V_{DD} - |V_{TP}|$ (or the source-gate voltage $V_{sgp} < |V_{TP}|$) driving all the associated transistors into the cut-off region (as visualised in grey in Fig. 2) and hence no output current is supplied. On the other side, V_{gp} is below its quiescent value enabling the transistors on this side to continue supplying the output current to the load Z_L. In effect, the class AB stage operates in a lateral manner where one side of the balanced output can supply the load current while the other side is off. When compared to the conventional push pull complementary MOS stage, this lateral class AB output has potential for a lower voltage operation since the minimum supply voltage requirement is not limited by the gate-source stacking of the conventional push-pull CMOS transistors.

Peak voltage swing: When the proposed OTA is employed in an active-RC or MOSFET-C filter, the maximum achievable peak differential output voltage $V_{out,max}$ can be derived based on strong inversion operation at large signal. Assuming that the filter employs a single resistive value of R and the OTA's input and output quiescent voltages are set at $V_{DD}/2$, $V_{out,max}$ is given by

$$V_{out,max} = V_{DD} + \left(\frac{1}{R \cdot \beta_P} + \frac{1}{R \cdot \beta_N}\right) - \sqrt{\frac{V_{DD}}{R \cdot \beta_P} + \frac{1}{(R \cdot \beta_P)^2}} - \sqrt{\frac{V_{DD}}{R \cdot \beta_N} + \frac{1}{(R \cdot \beta_N)^2}} \quad (1)$$

where $\beta_P = \mu_P C_{ox}(W/L)_P$ is the transconductance parameter of the pMOS amplifier (P3-P6) and $\beta_N = \mu_N C_{ox}(W/L)_N$ is that of the current mirror loads (N3-N6). Based on (1),

the dependence of the ratio $V_{out\,max}/V_{DD}$ on the product $R \cdot \beta = R \cdot \beta_P = R \cdot \beta_N$ and V_{DD} is shown as a contour plot in Fig. 3. The plot suggests that in order for the OTA to achieve the peak voltage swing close to V_{DD}, the product $R \cdot \beta$ should be made large. Since, for a given filter bandwidth ($\propto 1/RC$), the resistance R is normally determined by the required overall filter noise ($\propto 1/C$), β should be selected such that the $R \cdot \beta$ product is sufficiently large. Note, however, that too excessive β ($\propto$ W/L) may result in higher gate capacitances ($\propto$ WL) in the OTA's internal nodes with consequent bandwidth degradation.

3. Simulation Results

By employing the OTA of Fig. 1, a 5th-order 100 kHz elliptic active-RC filter, with the structure similar to the MOSFET-C filter design in [2], was simulated with Spectre using a 2-V 0.18 μm CMOS process (V_{TN} = 0.25 V, V_{TP} = −0.25 V). The transistor dimensions are as follows: N1-N2 = 150/2, N3-N6 = 20/0.3, No1-No4 = 20/1, No1-No4 = 10/0.6, P1-P2 = 15/3 and P3-P6 = 30/0.25. R_{SS} is at 50 kΩ and all the filter resistances R are at 500 kΩ. This together with $\beta = \beta_P = \beta_N$ = 1 mA/V^2 yields $R \cdot \beta$ = 500. At V_{DD} = 0.5 V, it is anticipated from (1) (or the plot of Fig. 3) that the available peak differential voltage swing is at 0.44 V_p which is as large as 88% of V_{DD}. Note that all the OTA's inside the filter shared the bias voltages V_{GB}, V_{DB} and V_{CB} that were generated from a single master bias circuitry to set the quiescent voltages $V_G = V_D$ = 0.25 V. At V_G = 0.25 V, the quiescent gate-source voltage of N1-N2 is at 0.15 V for the tail bias current through R_{SS} at 2 μA and the input differential pair operates near weak inversion.

Figure 4 shows the frequency responses of the filter under three different supply voltages. For the intended applications at 0.5-V, the filter exhibits the differential peak output of 0.42 V_p at less than 1% THD for the single-tone test ranging from 10 kHz to 90 kHz. For the simulated integrated noise at 158 μV_{rms}, this renders the signal-to-noise ratio (SNR) of 65 dB. Under the two-tone input test at 50 kHz and 55 kHz, the spurious-free dynamic range (SFDR) is at 60 dB. The filter's SFDR was also simulated at different two-tone inputs (from 10 kHz and 15 kHz up to 90 kHz and 95 kHz) for various supply voltages (0.5-V to 1.0-V), and the SFDR was found to be within the range of 56 dB to 66 dB. The whole filter including the bias circuitry consumes 100 μA.

The practicality of the cross-coupled biasing resistors was also confirmed by Monte-Carlo simulation where the standard deviation of both V_G and V_D, due to mismatches of No1-No4 and No1-No4, is within 5% of their corresponding quiescent voltages. Also, the filter shows no sign of instability when it is subjected to a rail-to-rail surge of the supply voltage (Fig. 5). The simulated SFDR and Figure-of-Merit (FoM), defined by power/(no. of poles × cut-off frequency × SFDR) [3] versus supply voltages are depicted in Fig. 6. The filter performances are summarised in Table 1.

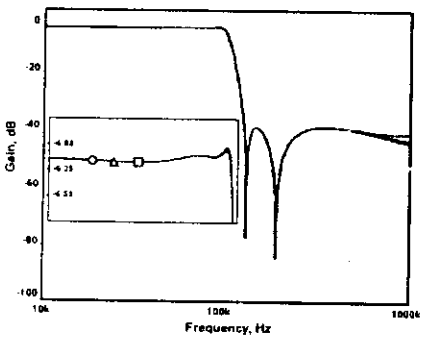

Fig. 4 Fifth-order elliptic filter frequency response with V_{DD}: ○ = 1.0 V, △ = 0.75 V, □ = 0.5 V.

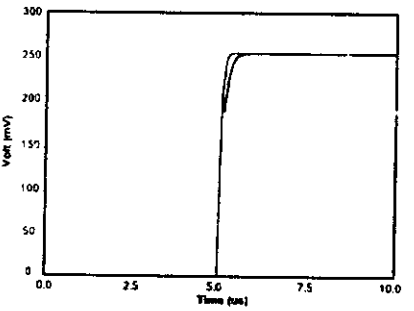

Fig. 5 Voltages of OTAs' inputs and outputs responded to a supply step change (from 0 V to 0.5 V).

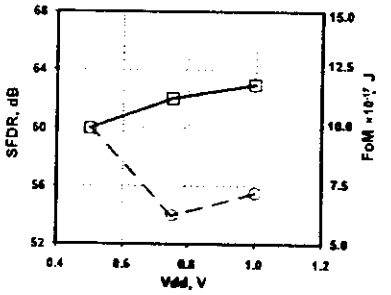

Fig. 6 Simulated SFDR, FoM versus V_{DD}: □ *SFDR*, ○ *FoM*.

Table 1 Summarised simulated filter performance.

Technology	0.18μm CMOS
Minimum supply voltage	0.5V
Filter type	5th-order Elliptic lowpass
Bandwidth	100kHz
SNR	65dB
SFDR	56dB
Power consumption	50μW

4. Conclusion

A compact OTA suitable for low voltage filter implementations has been developed. The circuit relies primarily on the feed-forward class AB output stage that features low supply operation and common-mode rejection at no cost to transconductance/bias-current efficiency. It is envisaged that the feed-forward output configuration could be applied to current-mode circuits in general or any other circuits with output current variables, such as transconductor (G_m), current conveyor etc. Verified through extensive simulation, it was demonstrated that a low supply voltage filter with a competitive FoM performance at small complexity is entirely viable with the use of the OTA structure.

Acknowledgments

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Structure of complex elliptic Gm-C filters suitable for fully differential implementation

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Abstract: The complexification method of Gm-C filters is presented. Unlike the previously reported method, the proposed method is suitable for the realisation of the fully differential complex Gm-C filters with finite zeros. Based upon the proposed method, complexification of the third-order elliptic Gm-C filter is demonstrated and the practical transistor-level simulation results of the resulting complex filter are also given.

1 Introduction

Much research work has been recently focused on the integrated low-IF receivers [1 - 7]. The principle of the low-IF receiver is closely related to that of the zero-IF receiver, and is based upon the use of quadrature mixing and complex filtering.

Frequency-shifting is a well-known method to transform a real filter into a complex filter. Frequency-shifted complex Gm-C filter can be realised by connecting each pair of the integrating nodes of two identical real filters with a pair of cross-coupled transconductors, as illustrated in Fig. 1. The frequency response of the complex filter is the linear frequency-shift version of the real filter prototype. However, the method shown in Fig. 1 is possible only for the case of the Gm-C filter without floating capacitor. Therefore it can be used to complexify only all-pole filters, for example Butterworth and Chebyshev filters, and not filters with finite zeros such as the elliptic filters.

The method that can be used to transform the single-ended real Gm-C filters with finite zeros into the corresponding single-ended complex Gm-C filters was introduced in [8], in which the essential elements were the quadratic imaginary resistors shown in Fig. 2*a*. Fig. 2*b* illustrates the quadratic realisation of the single-ended frequency-shifted capacitance obtained by shunting a pair of capacitors with the imaginary resistor in Fig. 2*a*. However, since the single-ended frequency-shifted capacitance in Fig. 2*b* is composed of two fully differential transconductors, it is not straightforward to convert this quadratic element into the fully differential structure.

In this paper, the state-space and element substitution methods to transform Gm-C filters, with or without floating capacitors, into complex filters are proposed. Both the proposed methods result in the single-ended complex Gm-C filter that employs only single-ended transconductor, a structure that can readily be converted into the fully differential circuit.

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2 Complexification of Gm-C filter using state-space technique

Consider the Gm-C filter in Fig. 3, which can be mathematically described as [9]

$$j\omega CV = GV + G_i V_i \tag{1}$$

where

$$V = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{bmatrix} \quad G_i = \begin{bmatrix} G_{1i} \\ G_{2i} \\ \vdots \\ G_{Ni} \end{bmatrix}$$

$$C = \begin{bmatrix} G_{11} & G_{12} & \cdots & G_{1N} \\ G_{21} & G_{22} & \cdots & G_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ G_{N1} & G_{N2} & \cdots & G_{NN} \end{bmatrix}$$

and

$$G = \begin{bmatrix} \sum_{j=0}^{N} C_{1j} & -C_{12} & \cdots & -C_{1N} \\ -C_{21} & \sum_{j=0}^{N} C_{2j} & \cdots & -C_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ -C_{N1} & -C_{N2} & \cdots & \sum_{j=0}^{N} C_{Nj} \end{bmatrix}$$

in which C_{j0} denotes grounded capacitor at node j, $C_{jk} = C_{kj}$ denotes floating capacitors connected between nodes j and k and $C_{jj} = 0$.

Using (1), the frequency responses of the filter can be expressed as

$$V = H(\omega)V_i$$

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{bmatrix} = \begin{bmatrix} H_1(\omega) \\ H_2(\omega) \\ \vdots \\ H_N(\omega) \end{bmatrix} V_i \tag{2}$$

where

$$H(\omega) = [j\omega C - G]^{-1} G_i \tag{3}$$

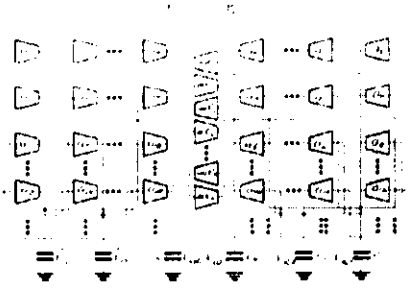

Fig. 1 *Complex Gm-C filter derived from real Gm-C filter without floating capacitor*

Without loss of generality, we consider the third-order ($N = 3$) complex filter in Fig. 4. Such a filter comprises a pair of real Gm-C filters connected to each other by an array of cross-coupled transconductors.

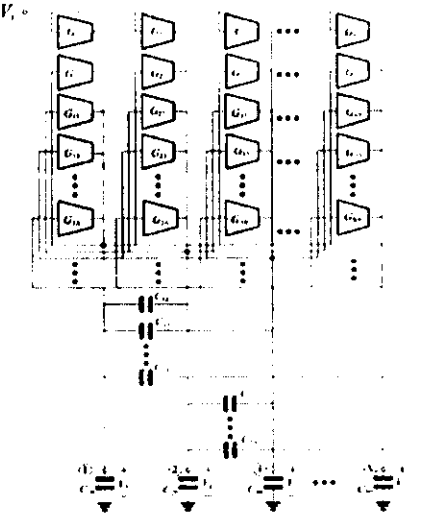

Fig. 3 *Structure of the Nth-order Gm-C filter*

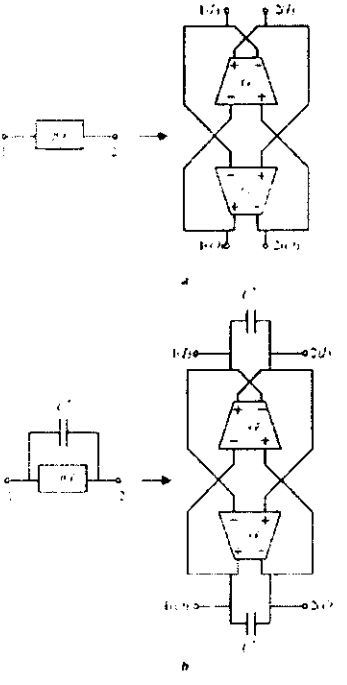

Fig. 2 *Quadratic (I and Q) realisation*

a Single-ended imaginary resistor
b Single-ended frequency-shifted capacitance employing a pair of differential transconductors with infinite CMRR [8]

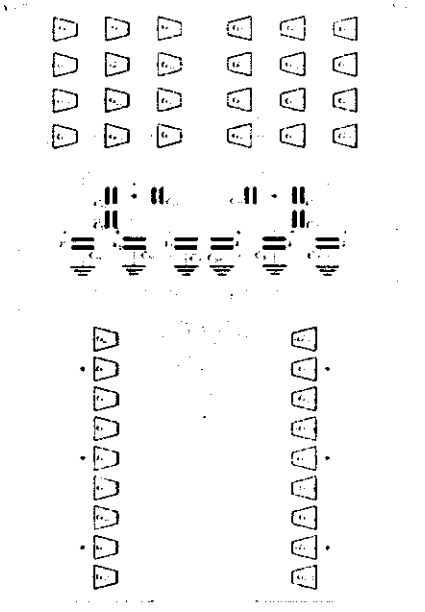

Fig. 4 *Third-order complex Gm-C filter*

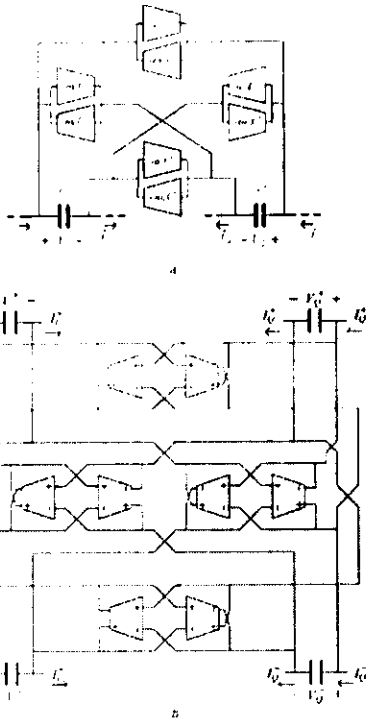

Fig. 5 *Quadratic realisation*
a Single-ended floating frequency-shifted capacitance
b Fully differential realisation

Referring to Fig. 4, for

$$G_o = \begin{bmatrix} G_{o11} & G_{o12} & \cdots & G_{o1N} \\ G_{o21} & G_{o22} & \cdots & G_{o2N} \\ \vdots & \vdots & \ddots & \vdots \\ G_{oN1} & G_{oN2} & \cdots & G_{oNN} \end{bmatrix}$$

we have

$$\begin{aligned} j\omega CV_I &= GV_I - G_oV_Q + G_iV_{i(I)} \\ j\omega CV_Q &= GV_Q + G_oV_I + G_iV_{i(Q)} \end{aligned} \tag{4}$$

where

$$V_I = \begin{bmatrix} V_{1(I)} \\ V_{2(I)} \\ \vdots \\ V_{N(I)} \end{bmatrix} \quad \text{and} \quad V_Q = \begin{bmatrix} V_{1(Q)} \\ V_{2(Q)} \\ \vdots \\ V_{N(Q)} \end{bmatrix}$$

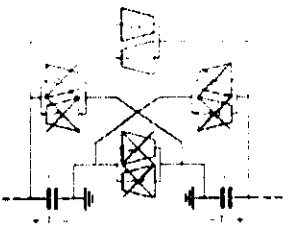

Fig. 6 *Single-end grounded frequency-shifted capacitance*

By defining $V_i = V_{i(I)} + jV_{i(Q)}$ and

$$V = \begin{bmatrix} V_{1(I)} \\ V_{2(I)} \\ \vdots \\ V_{N(I)} \end{bmatrix} + j \begin{bmatrix} V_{1(Q)} \\ V_{2(Q)} \\ \vdots \\ V_{N(Q)} \end{bmatrix}$$

the above equation can be re-written as

$$j\omega CV = GV + jG_oV + G_iV_i \tag{5}$$

According to (5), for

$$G_o = \omega_oC \tag{6}$$

it can be shown that

$$j\omega CV = GV + j\omega_oCV + G_iV_i \tag{7}$$

which leads to

$$V = H_S(\omega)V_i \tag{8}$$

where

$$H_S(\omega) = [j(\omega - \omega_o)C - G]^{-1}G_i \tag{9}$$

By comparing (9) and (3), it can be seen that the transfer function $H_S(\omega)$ can be expressed as

$$H_S(\omega) = H(\omega - \omega_o)$$

which is the linear shifted version of $H(\omega)$.

3 Complexification of Gm-C filter by element substitution technique

Fig. 5*a*, which is closely related to the frequency-shifted capacitance in Fig. 2*b*, illustrates that the frequency-shifted capacitance is composed of eight transconductors and a pair of floating capacitors. According to Fig. 5*a*, by defining the complex current and voltage variables as

$$I = I_I + jI_Q \text{ and } V = V_I + jV_Q$$

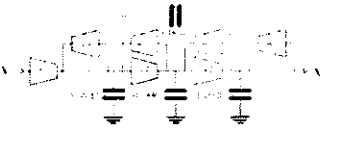

Fig. 7 *Third-order elliptic Gm-C filter ($\omega_o = G/C$) with 1.0 dB passband attenuation ($0 < \omega < \omega_p$) and 25 dB stopband attenuation ($\omega > 1.5\omega_p$)*

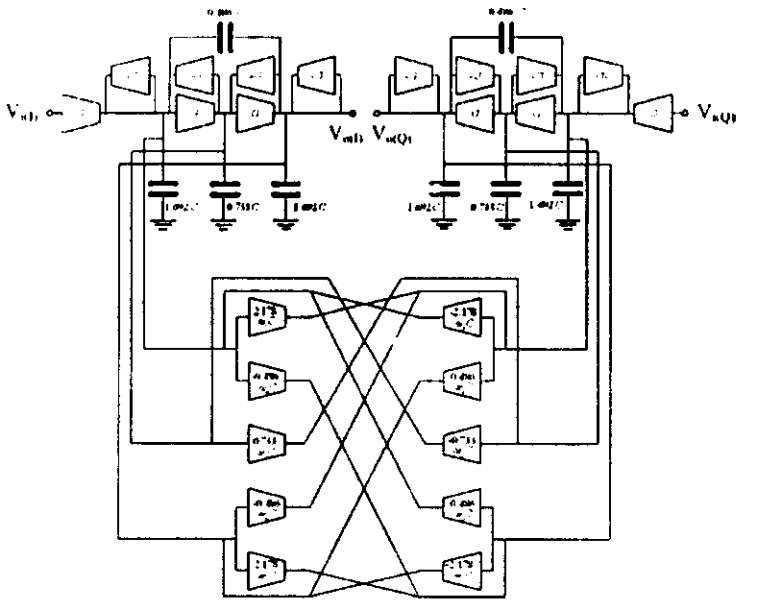

Fig. 8 *Complex Gm-C filter derived from the filter in Fig. 6 using state-space technique*

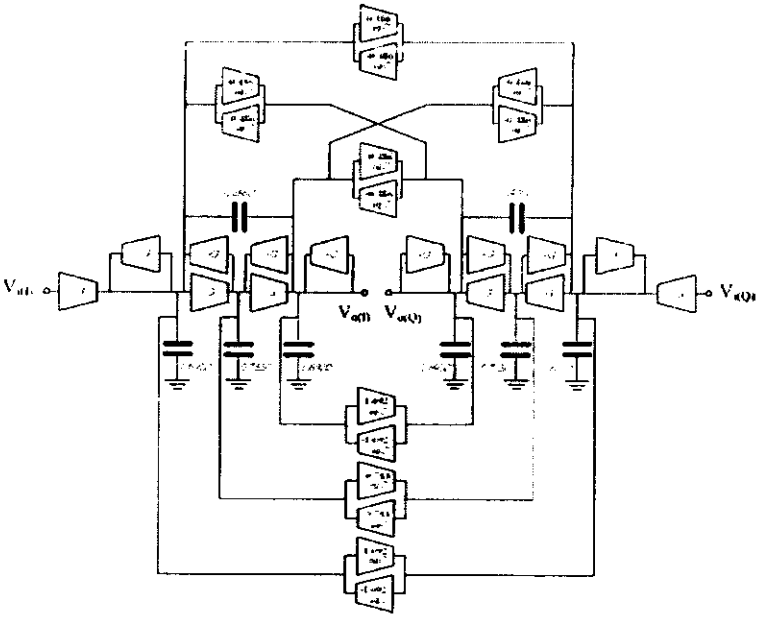

Fig. 9 *Complex filter obtained by connecting the I and Q sections in accordance with Figs. 5 and 6*

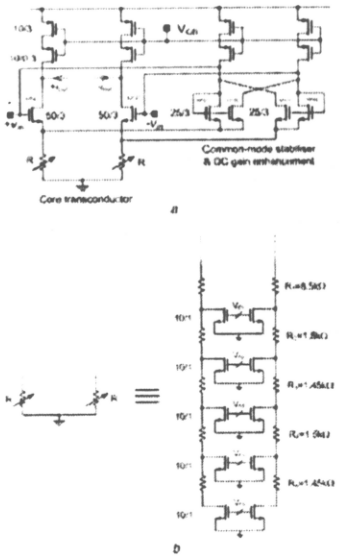

Fig. 10 *Transconductor and degeneration resistor*
a Transconductor with common-mode stabiliser and DC gain enhancement
b Implementation of the source degenerating resistor [11]

respectively, it can be shown that

$$I = j(\omega - \omega_0)CV \tag{10}$$

In other words, the effective admittance in Fig. 5*a* is $j(\omega - \omega_0)C$, which is the frequency-shifted version of the normal capacitive admittance. As a result, intuitively, linear frequency-shifted complex Gm-C filter can be realised by first doubling the real Gm-C filter prototype into two identical (I and Q) Gm-C sections, and then connecting each capacitor in the I section to its replica in the Q section with the transconductance network shown in Fig. 5*a*. The fully differential realisation of the frequency-shifted capacitance in Fig. 5*a* is depicted in Fig. 5*b*. It is worth noting that in the case of grounded capacitors, the network in Fig. 5*a* can be reduced to the one as shown in Fig. 6, which corresponds to the conventional complex filter structure in Fig. 1.

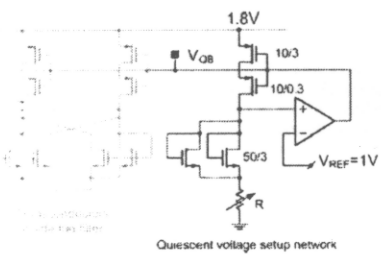

Fig. 11 *Quiescent-voltage setting up network for the filter*

4 Design example

According to (1), the matrices that correspond to the elliptic filter in Fig. 7 are

$$G = \begin{bmatrix} -G & -G & 0 \\ G & 0 & -G \\ 0 & G & -G \end{bmatrix}, \quad G_i = \begin{bmatrix} G \\ 0 \\ 0 \end{bmatrix}$$

and

$$C = \begin{bmatrix} 2.178C & 0 & -0.486C \\ 0 & 0.733C & 0 \\ -0.486C & 0 & 2.178C \end{bmatrix}$$

Consequently from (6), we have

$$G_o = \begin{bmatrix} 2.178C\omega_o & 0 & -0.486C\omega_o \\ 0 & 0.733C\omega_o & 0 \\ -0.486C\omega_o & 0 & 2.178C\omega_o \end{bmatrix}$$

According to the above matrices, the complex filter derived from the real Gm-C filter of Fig. 7 is shown in Fig. 8, which is a single-ended structure that can be readily converted into fully differential realisation.

Alternatively, by doubling the Gm-C filter in Fig. 7 into I and Q sections and connecting each capacitor in the I section to its respective duplicated capacitor in the Q section with the transconductance network shown in Fig. 5*a* (in the case of floating capacitors) and Fig. 6 (in

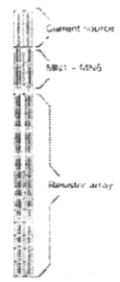

Fig. 12 *Layout of the transconductor of Fig. 10*

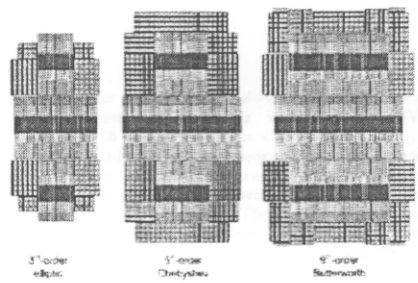

Fig. 13 *Layouts of the complex Gm-C filters*

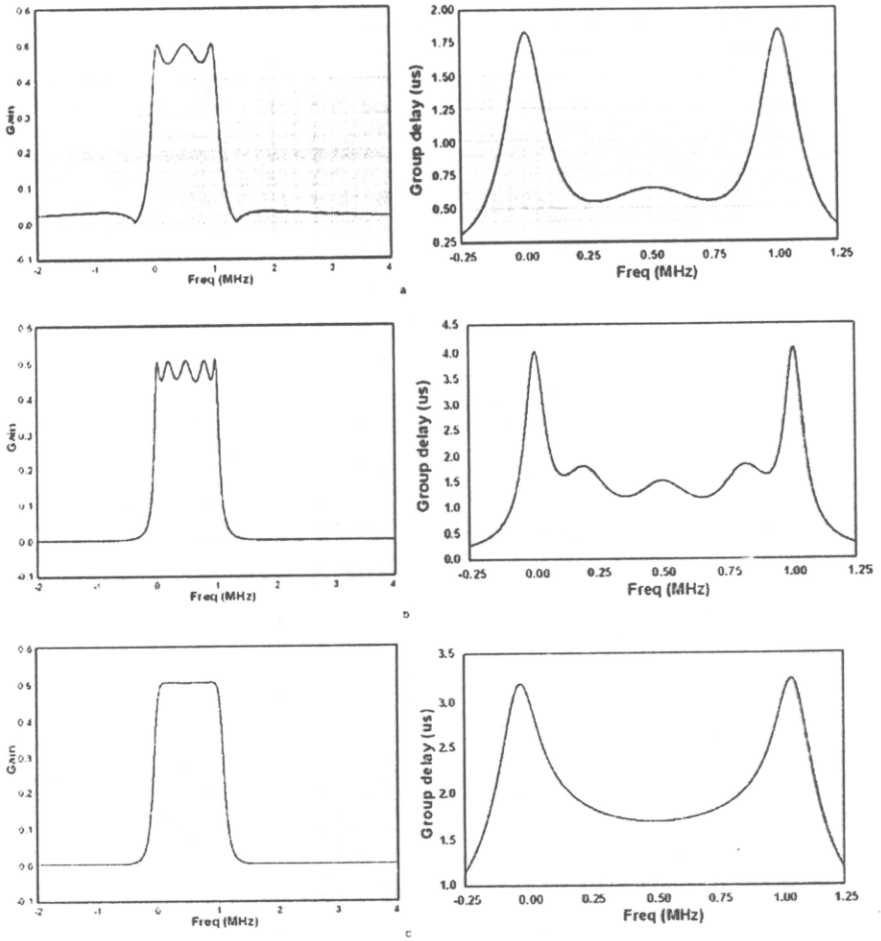

Fig. 14 *Simulated AC simulation results (magnitude and inband group delay) of the complex filters*

a Third-order elliptic filter
b Fifth-order Chebyshev filter
c Ninth-order Butterworth filter

the case of grounded capacitors), the complex filter in Fig. 9 is obtained. It is straightforward to show that by combining all the transconductors that are connected in parallel together, the complex filter in Fig. 9 becomes identical to the complex filter in Fig. 8.

5 Transistor-level filter simulation

A practical complex filter has also been designed and simulated based on the proposed Gm-C complexification concept. The differential version of the complex filter shown in Fig. 8 has been implemented such that the resulting filter possesses a bandwidth of 1 MHz and a centre frequency of 500 kHz with $G = 20\ \mu A/V$, $C = 6.37 \times 10^{-12}$ F and $\omega_o = 2\pi \times 500$ krad/s.

As illustrated in Fig. 10, the transconductor employed in the design is the pseudo-differential resistive source-degeneration type [10, 11] connected with the common-mode stabilising network [12]. The degeneration resistor R can be tuned using a network of linear resistors in series with triode-MOS resistors (Fig. 10*b*) similar to what has been proposed in [11]. Filter tuning can be achieved by adjusting gate voltage of the triode-MOS resistor following the same technique presented in [11].

Table 1: Performance comparison of complex filter

Derived from	Third-order elliptic	Fifth-order Chebyshev	Ninth-order Butterworth
Technology	0.18 μm CMOS		
Supply voltage	1.8 V		
Output noise integrated from 1 Hz to 10 MHz (V^2)	1.96×10^{-7}	2.96×10^{-7}	3.63×10^{-7}
Spurious-free dynamic range (dB)	47.1	44.6	43.3
1%-IM3-DR (dB)	50.1	46.8	44.7
Total integrating capacitance (pF)	117.2	240.7	272.0
Total number of unit Gm's	32	48	66
Power consumption (static) (mW)	1.64	2.14	3.01
Current consumption (static) (mA)	0.86	1.19	1.67
Area (mm^2)	0.72	1.22	1.59

Transistors employed in the common-mode stabilising network have also been appropriately sized to enhance DC-gain. All the transconductors are biased by simple cascode PMOS current sources whose gate voltage V_{QB} is set by a single network of Fig. 11, where transconductor's input and output quiescent voltages are set to be equal to V_{REF}. Two diode-connected MOS ($W/L = 50\ \mu m/3\ \mu m$) emulate the fact that under a quiescent condition, transistors MN1–MN2 and MN3–MN6 in the common-mode stabilising network resemble a diode-connected NMOS. In this design, the quiescent DC voltage is set to be at 1 V.

The complex third-order elliptic filter derived from the proposed method is compared to the complex filters with the same frequency specifications, namely the fifth-order Chebyshev and the ninth-order Butterworth filters. As the real Butterworth and Chebyshev filters do not have finite transmission zero, they can be transformed to complex filters by the conventional method (Fig. 1). Based on the layout of the unit transconductance cell in Fig. 12 and with capacitive trimming, by taking into account parasitic capacitances, the layouts of the three filters under considerations are depicted in Fig. 13. It is clear from Fig. 13 that the proposed elliptic filter occupies much smaller area than the Chebyshev and Butterworth filter counterparts. Simulations with parasitic capacitances extracted from the layouts have been conducted using Spectre with Cadence design suite employing 3.3 V 0.18 μm CMOS process under 1.8 V (PMOS and NMOS threshold voltages are ~0.45 V) supply. Simulations results have been obtained by injecting quadrature signals into the circuits. Simulated AC responses (magnitude and inband group delay) of all the filters are shown Fig. 14. Other filter performances including the spurious-free dynamic range, 1% third-order intermodulation-dynamic range (1%-IM3-DR), total capacitance and total transconductors employed, power and current consumption are listed in Table 1. It can be observed from Table 1 that with the same frequency specifications, the proposed complex elliptic Gm-C filter is more linear, has better noise performance, requires less chip area and consumes less power than the complex Butterworth and Chebyshev Gm-C filters.

6 Conclusion

We have presented two different methods, based on state-space and element substitution, to transform the real Gm-C filters with floating capacitors into the corresponding complex Gm-C filters. The resulting complex filter structure is suitable for fully differential implementation using widely used fully differential transconductors. To demonstrate the proposed method, the fully differential complex Gm-C filter was realised from the third-order elliptic Gm-C filter. It was found that with the same frequency specifications, the elliptic complex filter derived from the proposed method outperforms the Butterworth and Chebyshev complex filters in terms of noise, linearity, area and power consumption.

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